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IBM Customer Engineering

Instructional Logic Diagrams

1410 Data Processing System

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Instructional Logic Diagrams

1410 Data Processing System

This book is designed primarily for instruction purposes. It shows the major logic of the 1410 system, but does not contain all the circuits shown in the ALD's. The ILD's were drawn from second levels contained in existing manuals of instruction and from ALD's with an EC number of 253259. There will be no revision to this manual.

The ILD's are organized throughout CPU by functional unit while the I/O areas are shown by sequence of operation.

All ILD's that have a figure number with the suffix A or B are functional "big pictures" which show the individual Data and Control ILD's for specific functional units.

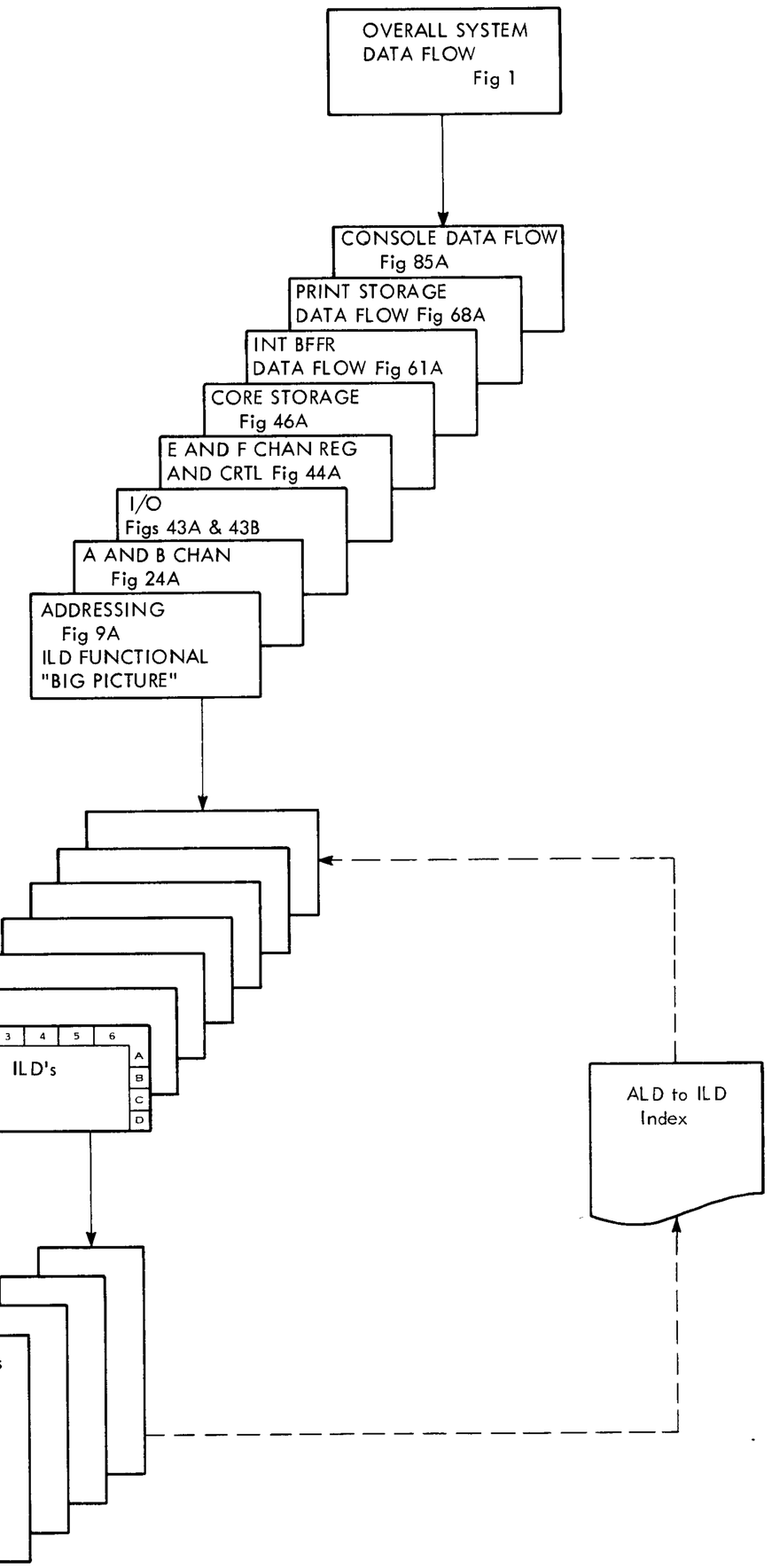
The normal usage path would be from Overall Data Flow to functional "big picture" then to the individual ILD and ultimately to the ALD.

An ALD/ILD Index follows the ILD's. It is arranged in numerical sequence by ALD page number to aid in returning to the ILD's from the ALD's. ILD lines are referenced using a co-ordinate system as follows:

25 D 2

The first number (25) represents the ILD figure number from which or to which the line is referenced. The alphabetic character (D) represents the vertical position on the figure while the last number (2) represents the horizontal position.

The ILD output lines are indexed to the ILD page on which they appear in a listing found after the ILD/ALD index.



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68	Print Control and Print Bfr Rings
69	Print Controls
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85	Console Control
86	Cons Matrix
87	Cons Start-Stop
88	Cons Function Ctrl
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90	Cons Read-Write Op
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184	TAU Read Controls II
185	TAU Unit Control
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187	TAU Delay Counter
188	TAU RDD, FSD and Check Character
189	TAU Go and Tape Drive Inputs
190	TAU Final Amplifiers
191	TAU Error Circuits I
192	TAU Error Circuits II
T80	Tape Unit Response Logic

1410 Intermediate Logic Diagrams

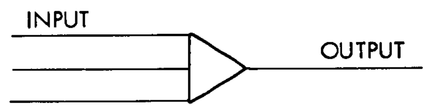
1-43	CPU
44-46	Channel
47-50	Core
51-57	1401 Compatibility
58-60	Master Error and Control
61-71	1414-3 (RD-PCH, PRT)
85-91	1415 Console
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Data Flow

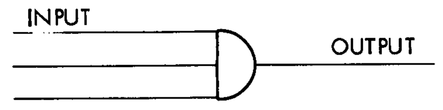
9A	Addressing
24A	A and B Channels
43A	Input/Output Data Flow
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44A	E Chan Reg and Controls (RDR)
46A	Core Storage
61A	Int Bfr Data Flow
68A	Print Stor Data Flow
85A	Console Data Flow and Control

SYMBOLOGY USED THROUGHOUT 1410 INTERMEDIATE LOGIC DIAGRAMS

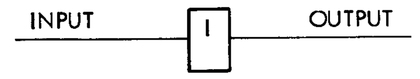
AND CIRCUIT

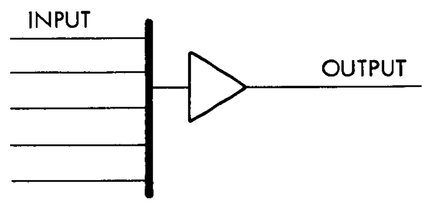


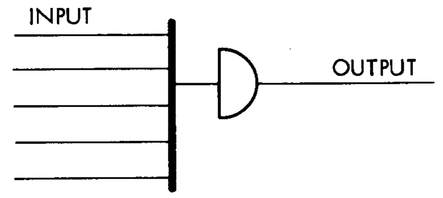
OR CIRCUIT



FUNCTIONAL INVERTER



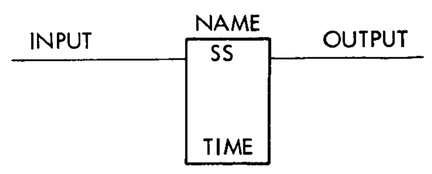




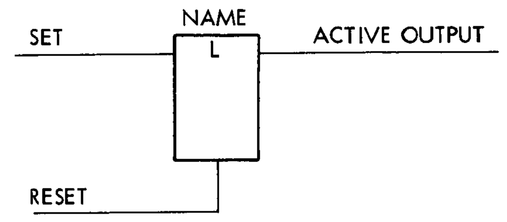
INDICATOR



SINGLE SHOT



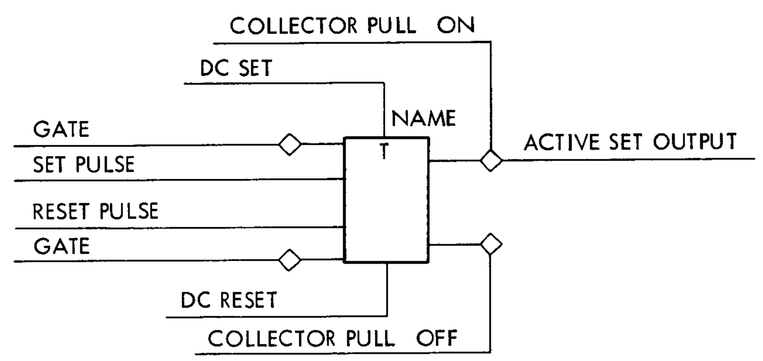
LATCH



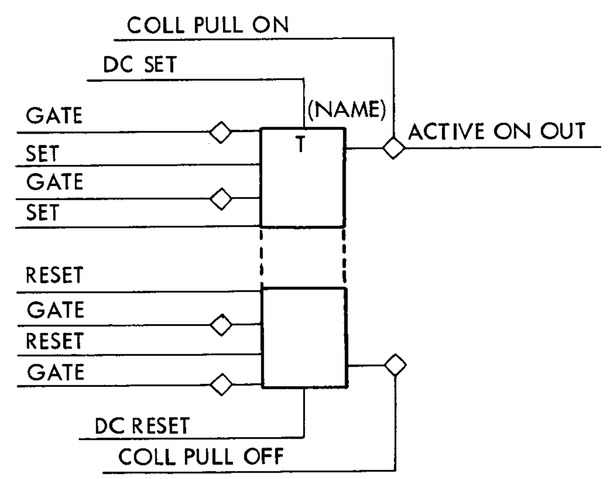


CHANGE LINE NAME ONLY

TRIGGER



DOUBLE SET/RESET TRIGGER

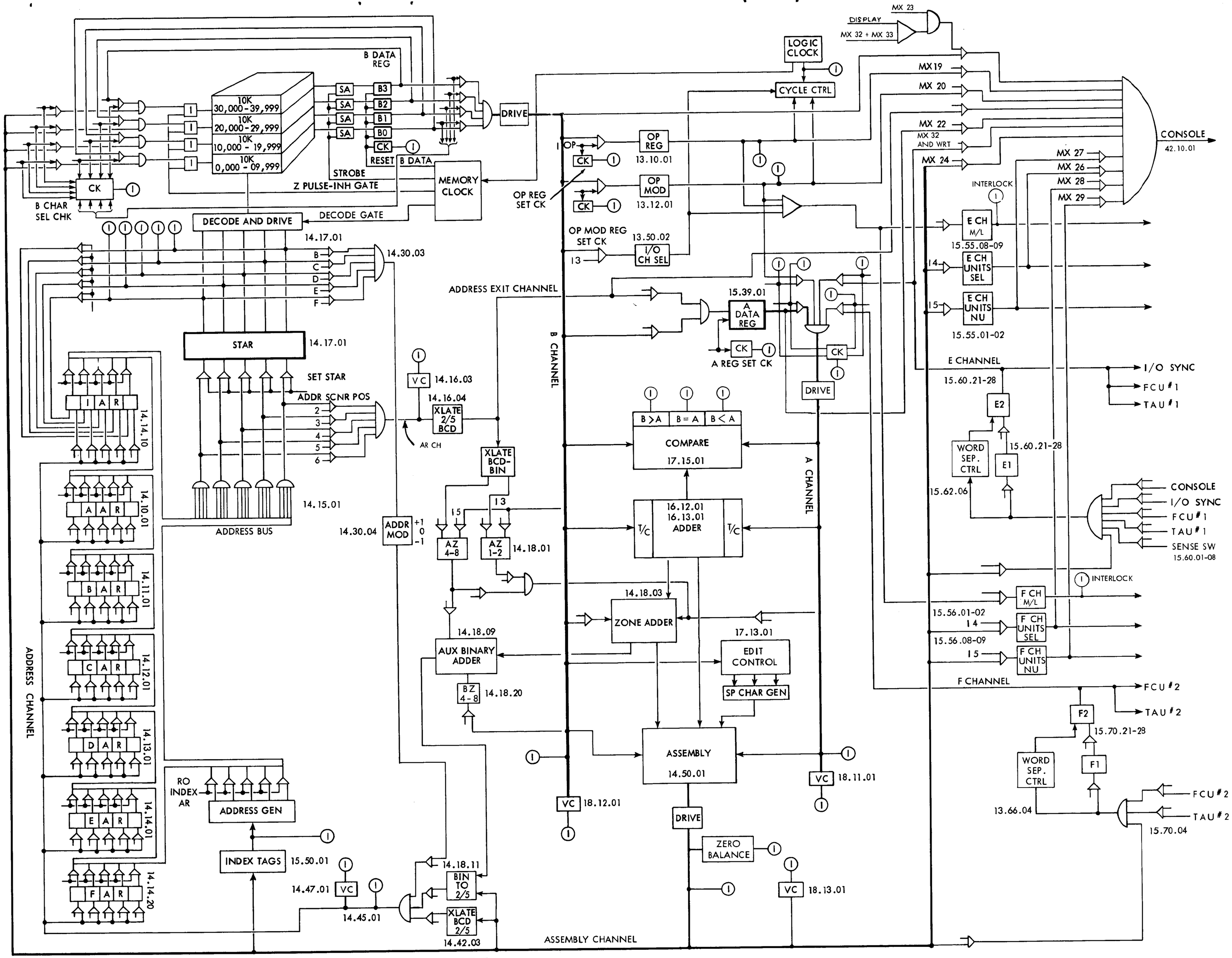


NOTES:

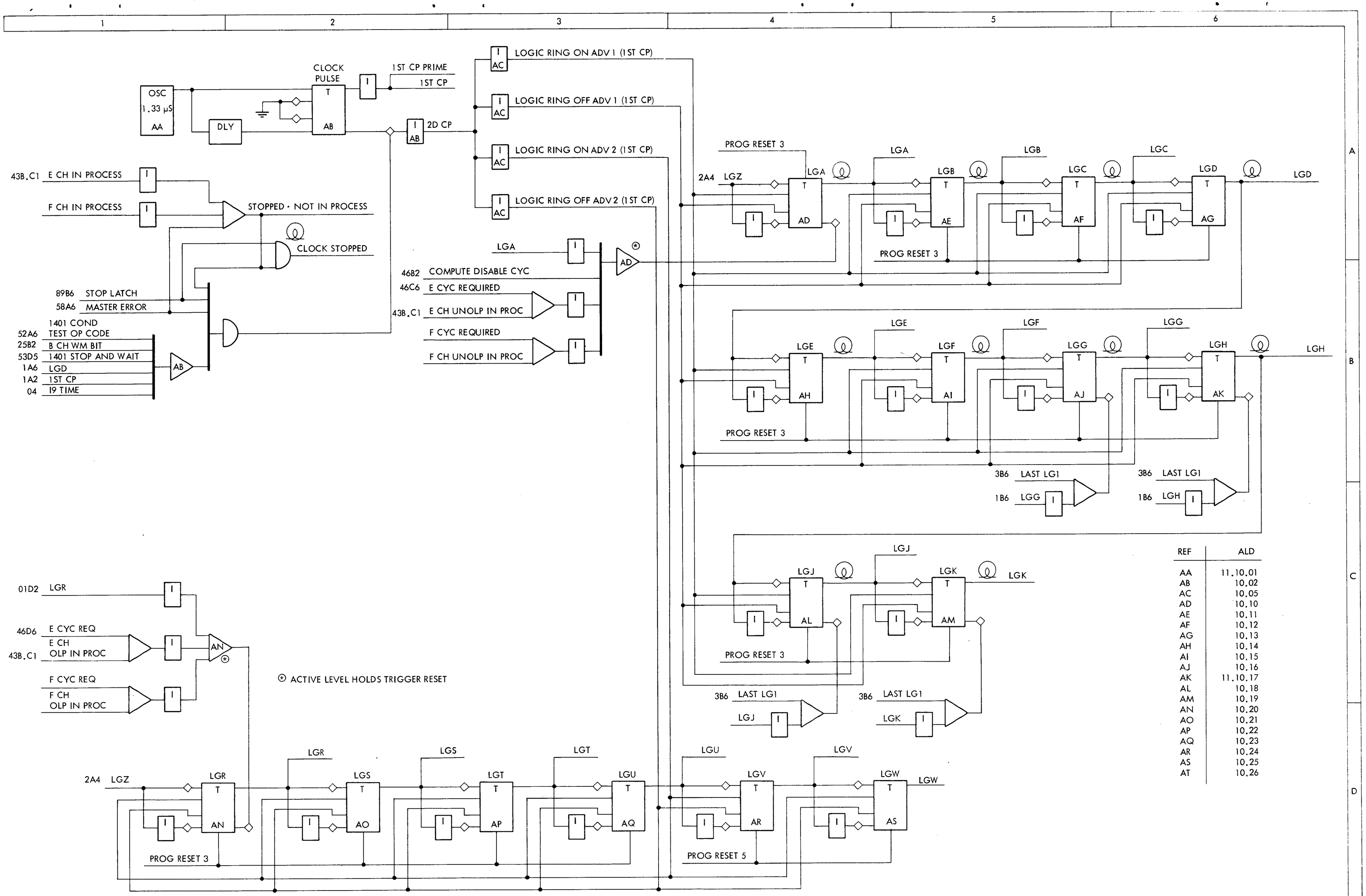
ALL NAMES ENCLOSED IN PARENTHESES ARE FOR LOGICAL EXPLANATION AND DO NOT NECESSARILY APPEAR IN THE ALD'S

ANY ASTERISKS SHOWN ARE AN ACTUAL PART OF THE ALD LINE NAME

ALL CONDENSED LOGIC DIAGRAMS ARE POSITIVE LOGIC THROUGHOUT

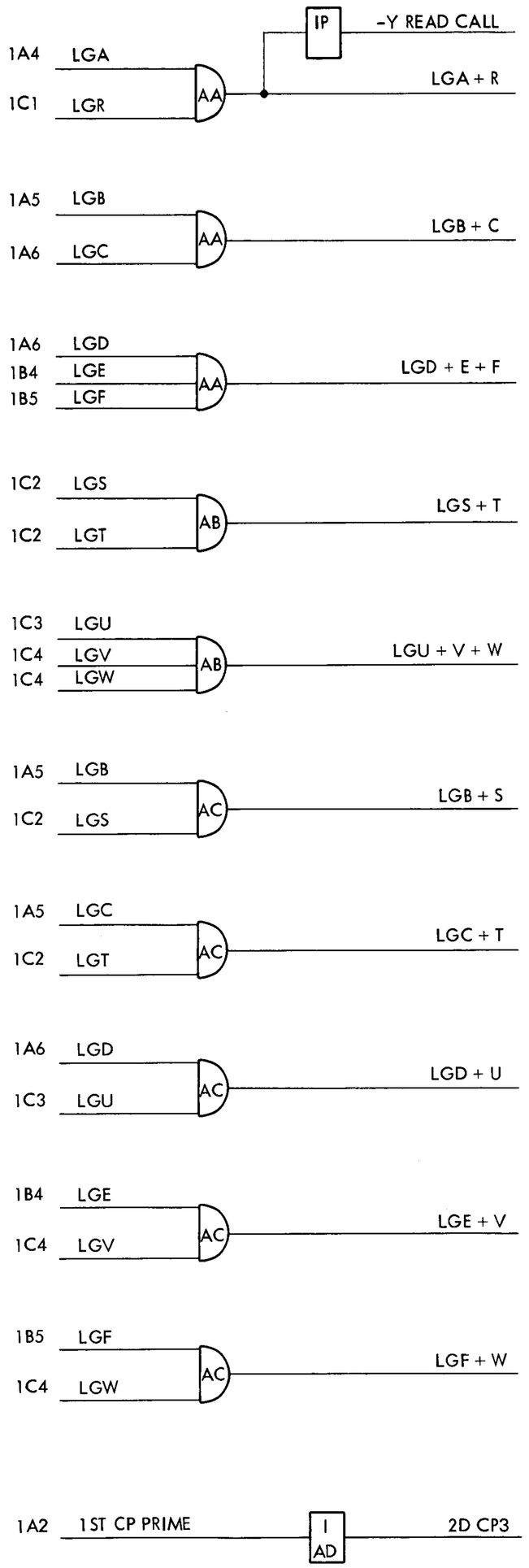


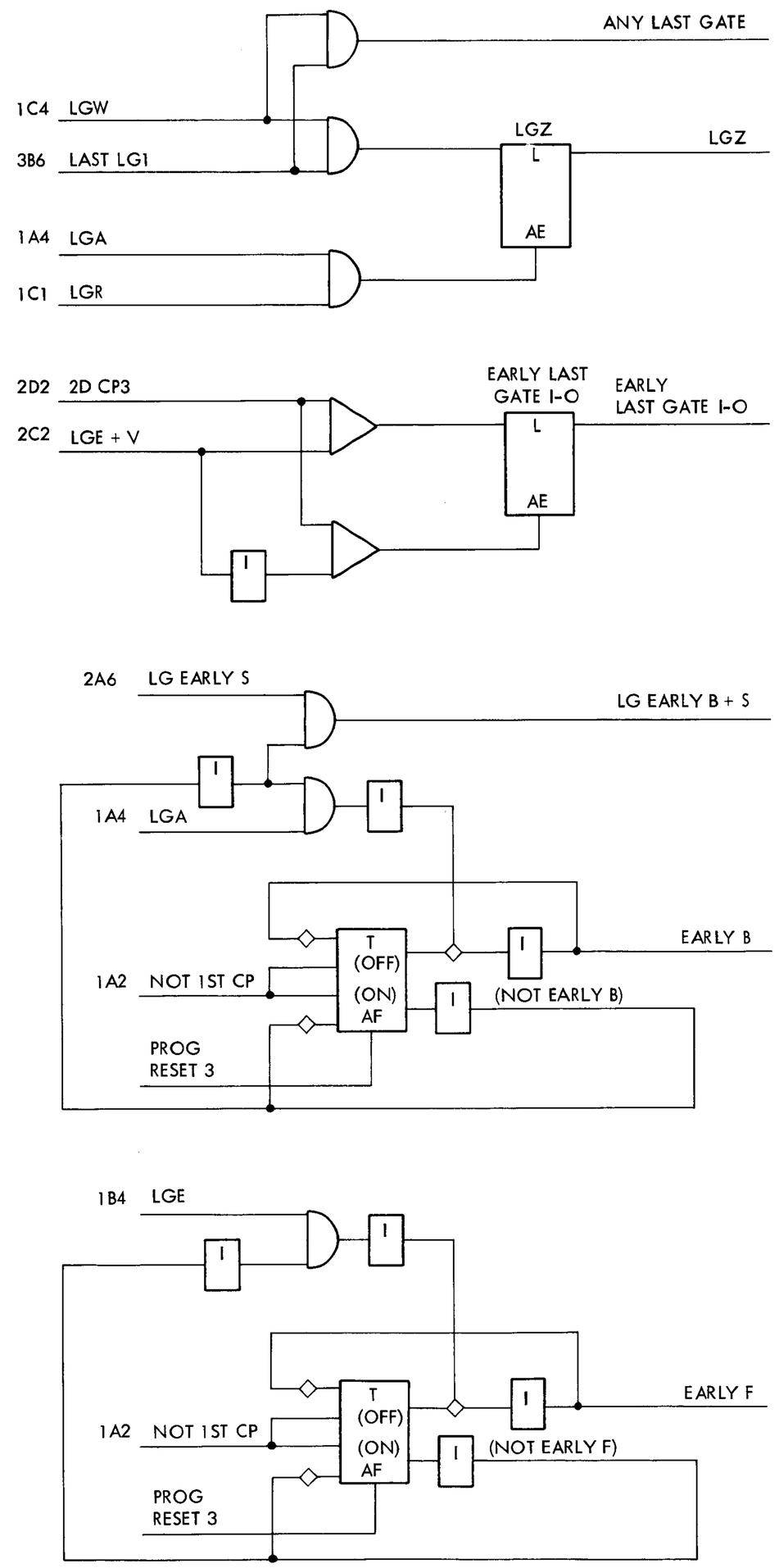
IBM 1410 Data Processing System Data Flow

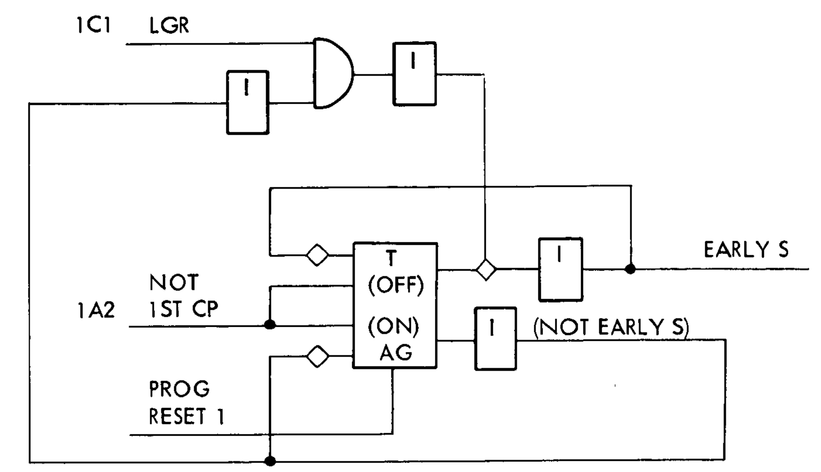


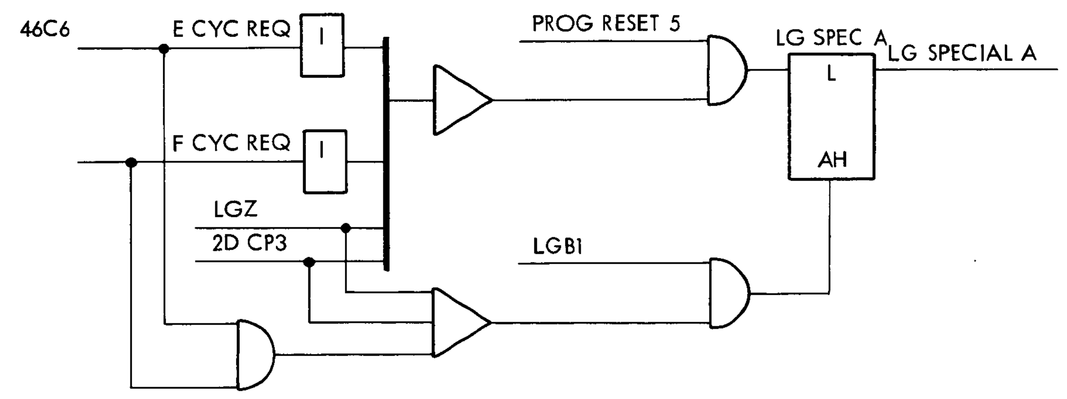
REF	ALD
AA	11.10.01
AB	10.02
AC	10.05
AD	10.10
AE	10.11
AF	10.12
AG	10.13
AH	10.14
AI	10.15
AJ	10.16
AK	11.10.17
AL	10.18
AM	10.19
AN	10.20
AO	10.21
AP	10.22
AQ	10.23
AR	10.24
AS	10.25
AT	10.26

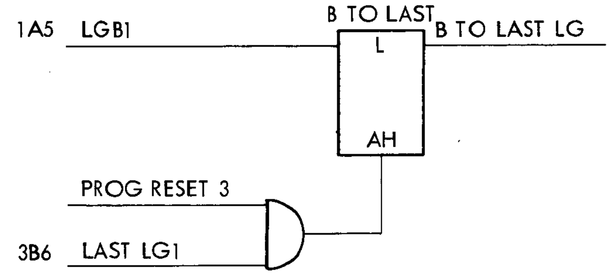
FIGURE 1. CLOCK, LOGIC RING, AND LOGIC RING EXTENSION







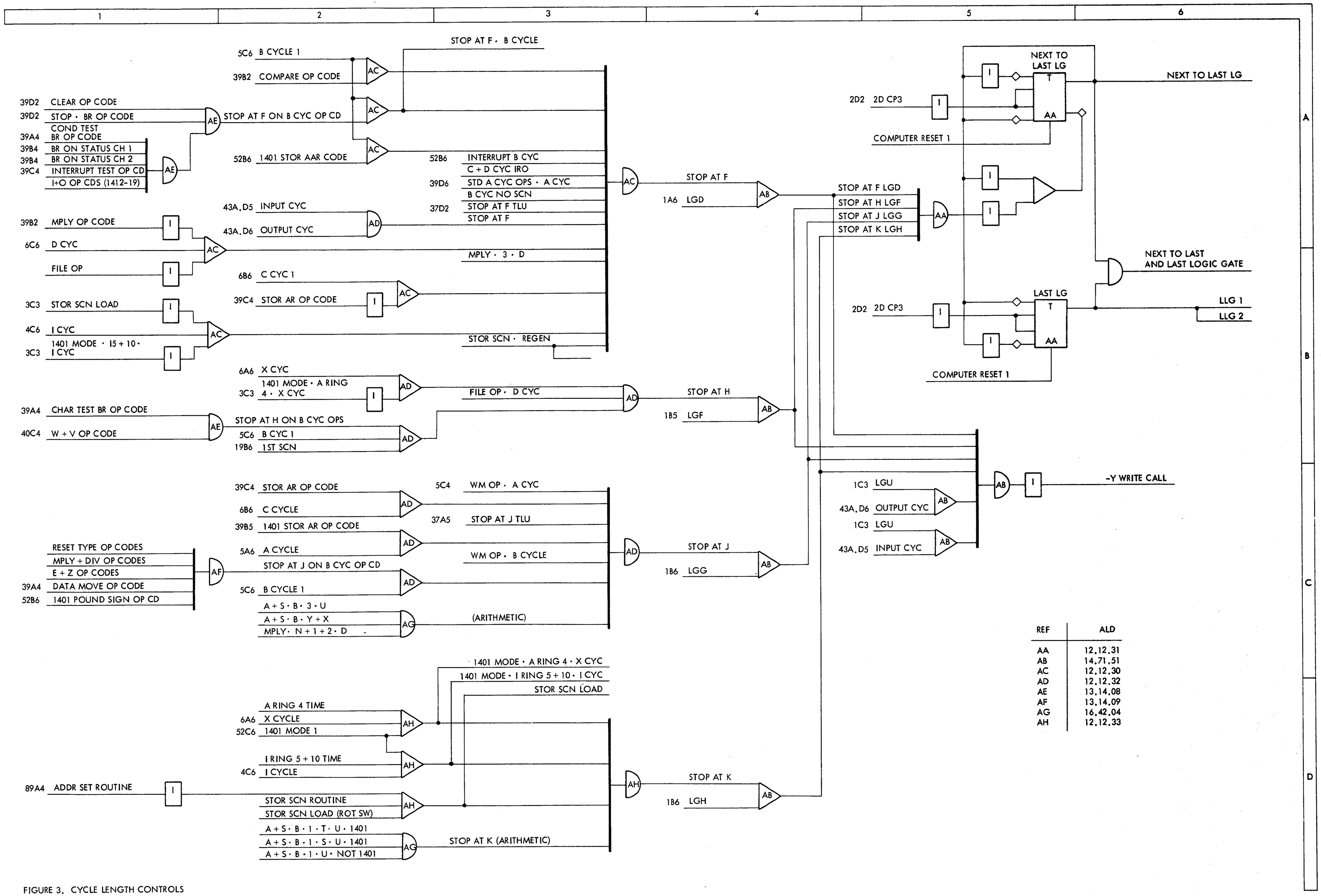




REF	ALD
AA	11.10.32
AB	10.33
AC	10.34
AD	10.36
AE	10.06
AF	30.01
AG	30.03
AH	30.02

NOTE: ALL PARENTHESISED NAMES ARE FOR REFERENCE PURPOSES ONLY

FIGURE 2. LOGIC GATE MIX AND SPECIAL LOGIC GATES



REF	ALD
AA	12.12.31
AB	14.71.51
AC	12.12.30
AD	12.12.32
AE	13.14.08
AF	13.14.09
AG	16.42.04
AH	12.12.33

FIGURE 3. CYCLE LENGTH CONTROLS

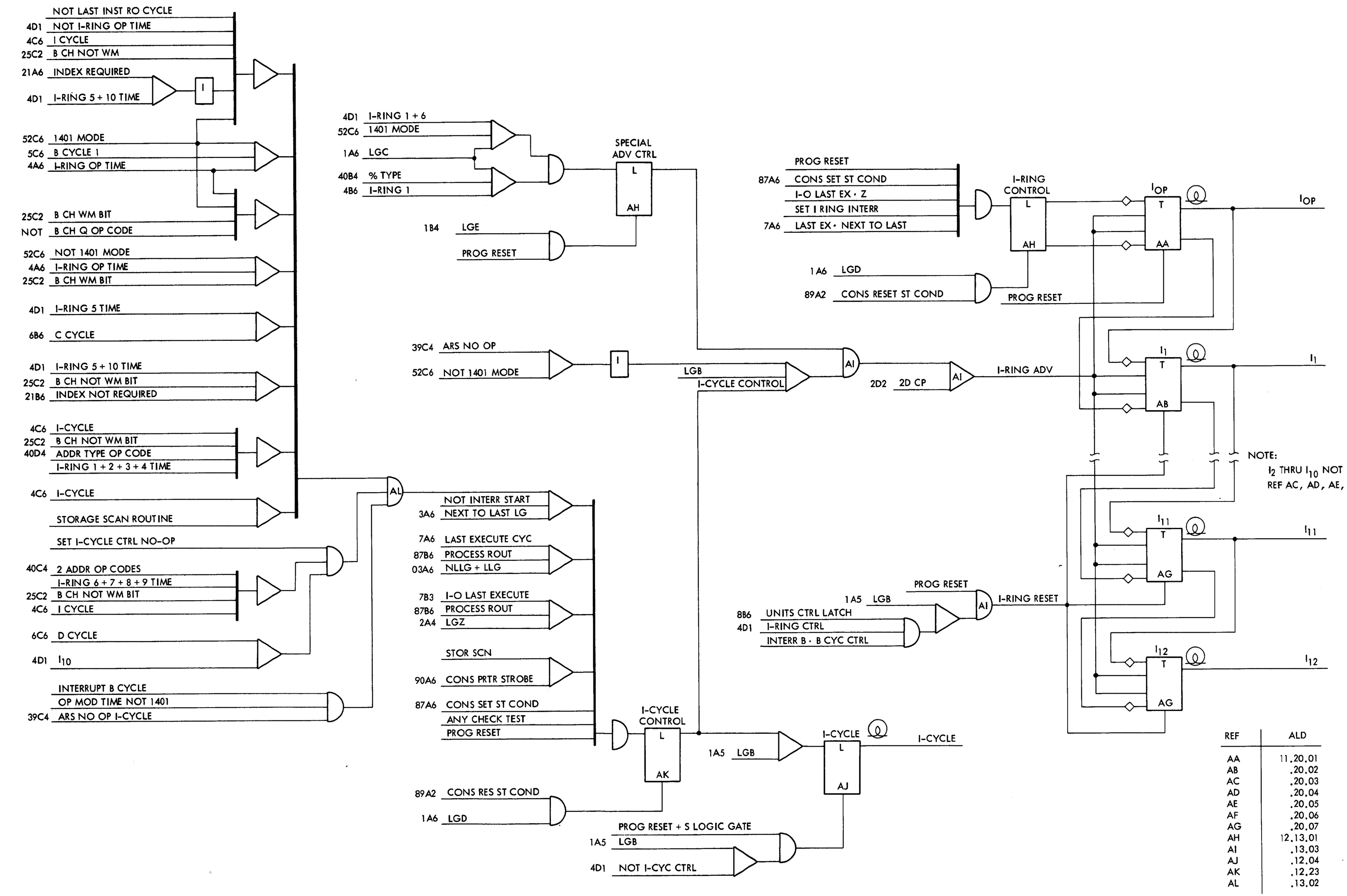


FIGURE 4. I CYCLE CONTROL AND I RING

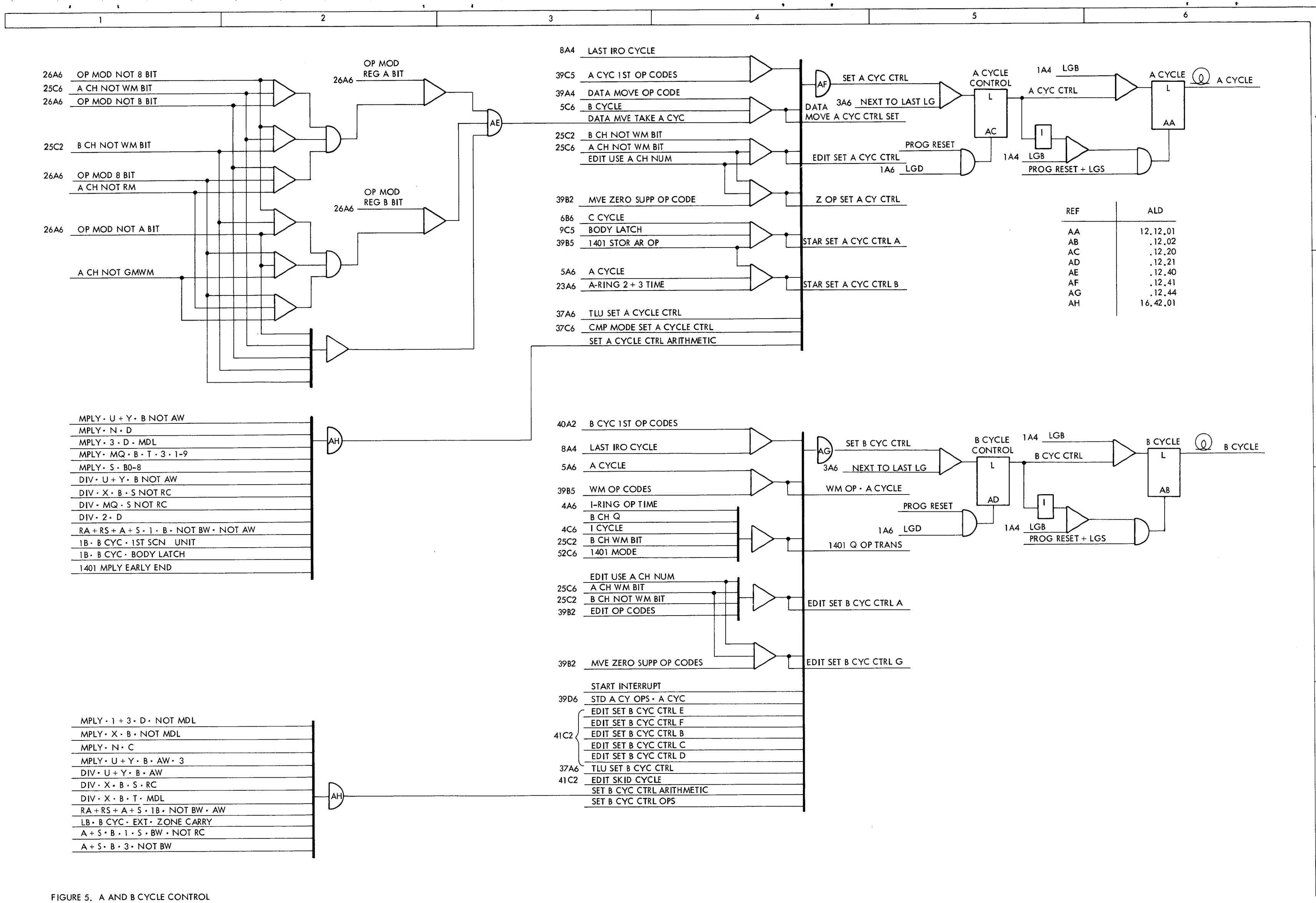
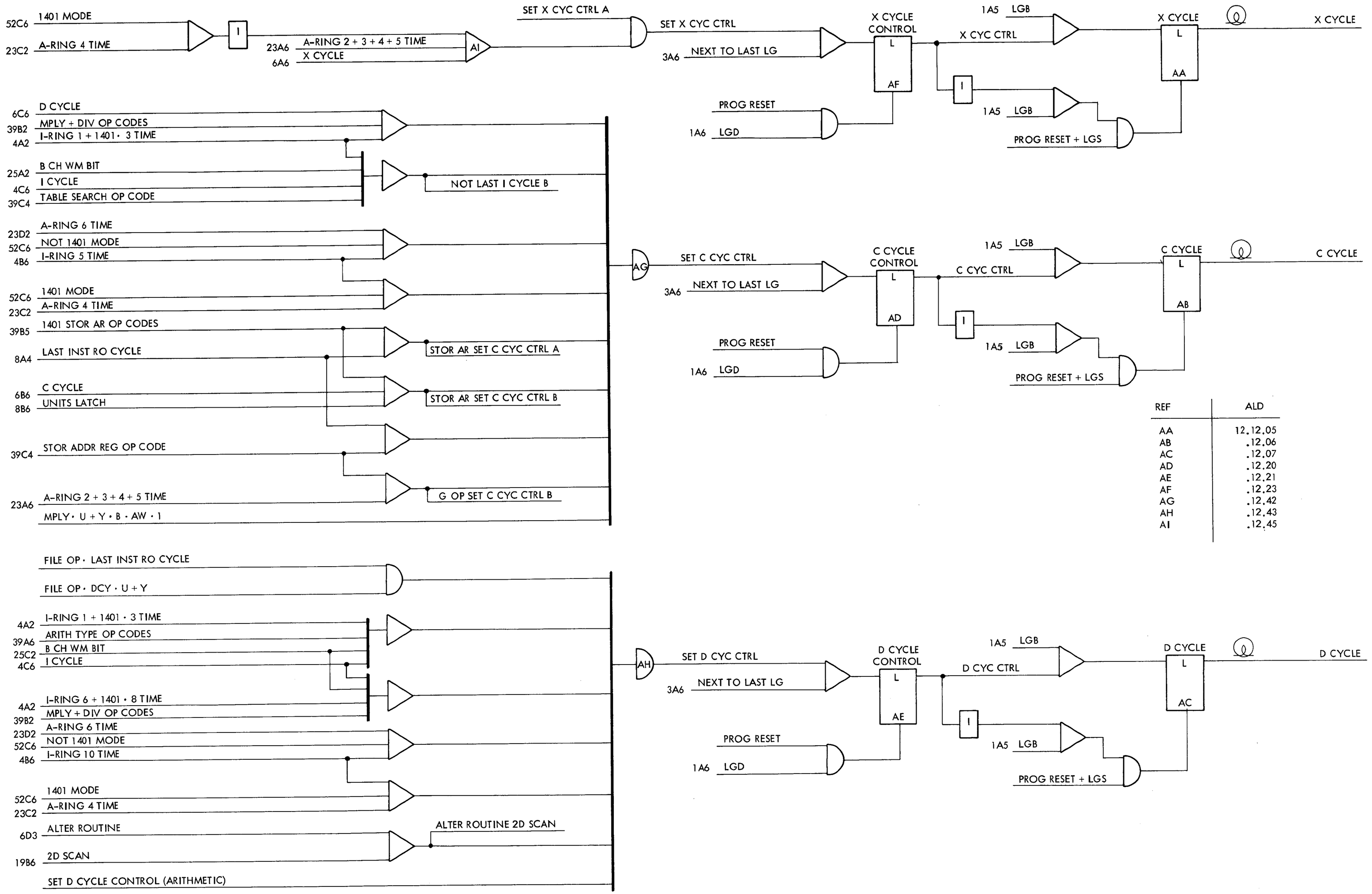
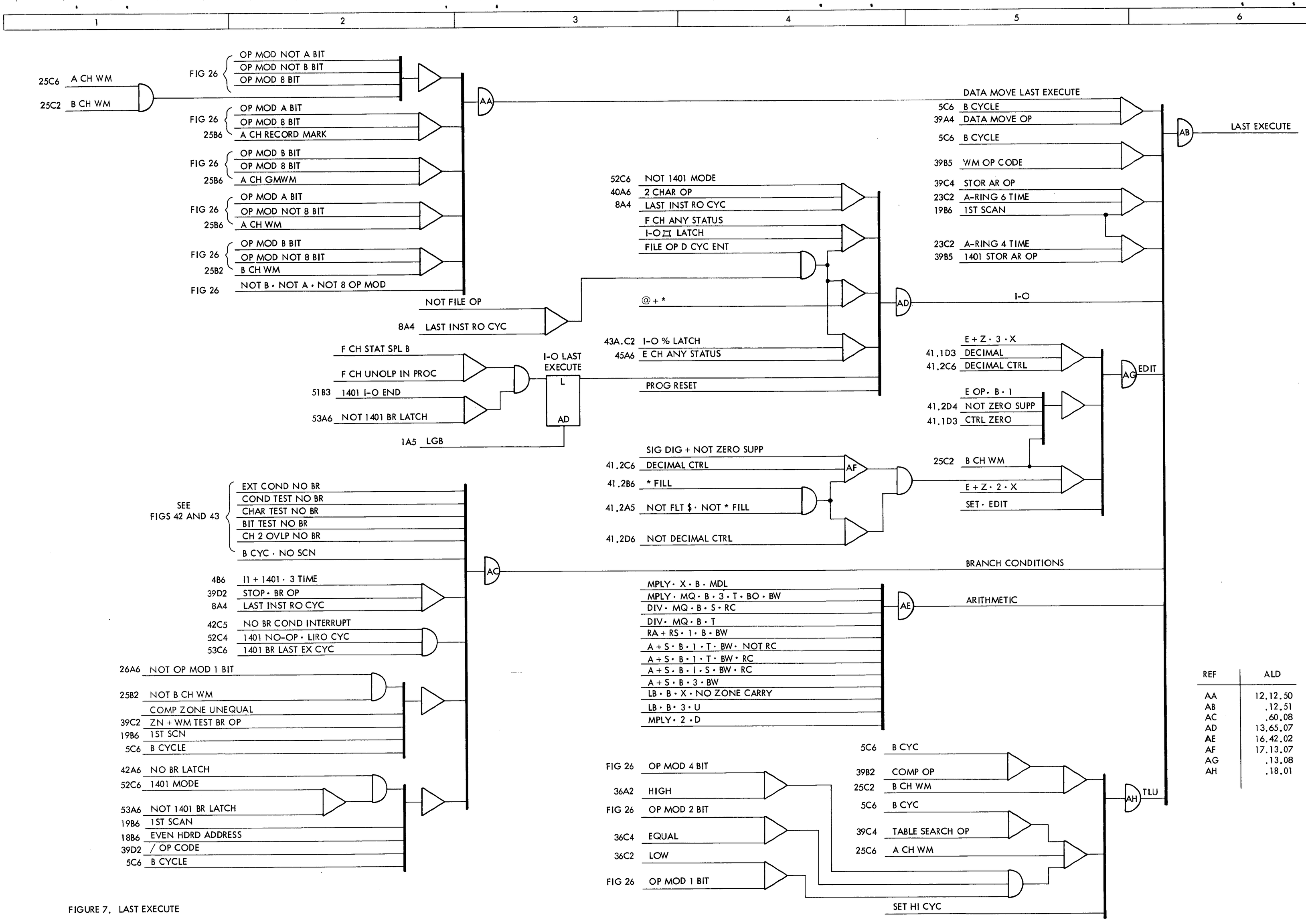


FIGURE 5. A AND B CYCLE CONTROL



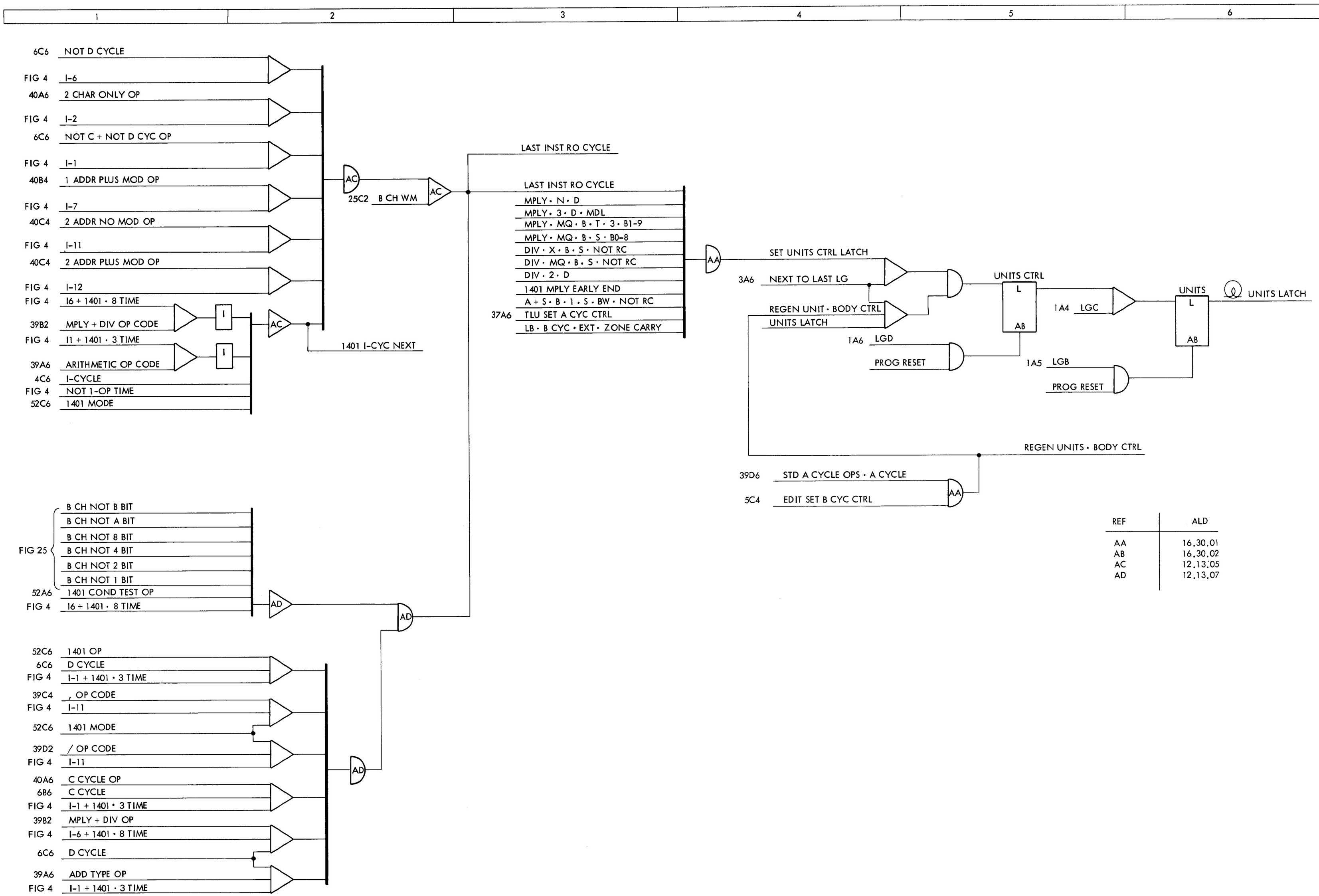
REF	ALD
AA	12.12.05
AB	.12.06
AC	.12.07
AD	.12.20
AE	.12.21
AF	.12.23
AG	.12.42
AH	.12.43
AI	.12.45

FIGURE 6. X, C, AND D CYCLE CONTROL



REF	ALD
AA	12.12.50
AB	.12.51
AC	.60.08
AD	13.65.07
AE	16.42.02
AF	17.13.07
AG	.13.08
AH	.18.01

FIGURE 7. LAST EXECUTE



REF	ALD
AA	16.30.01
AB	16.30.02
AC	12.13.05
AD	12.13.07

FIGURE 8. LAST INST RO, UNITS CTRL, AND LATCH

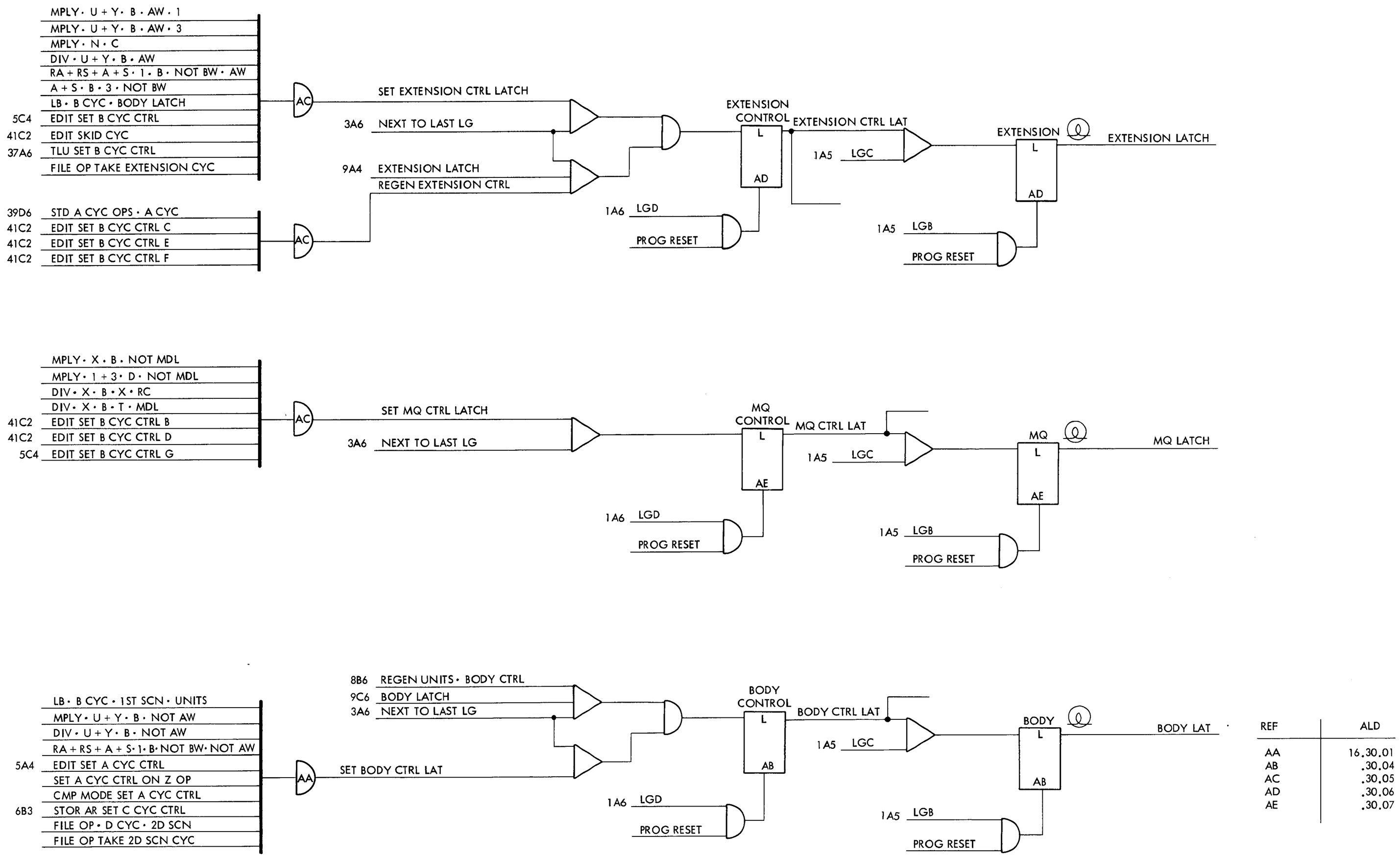


FIGURE 9. BODY, EXTENSION, MQ LATCH

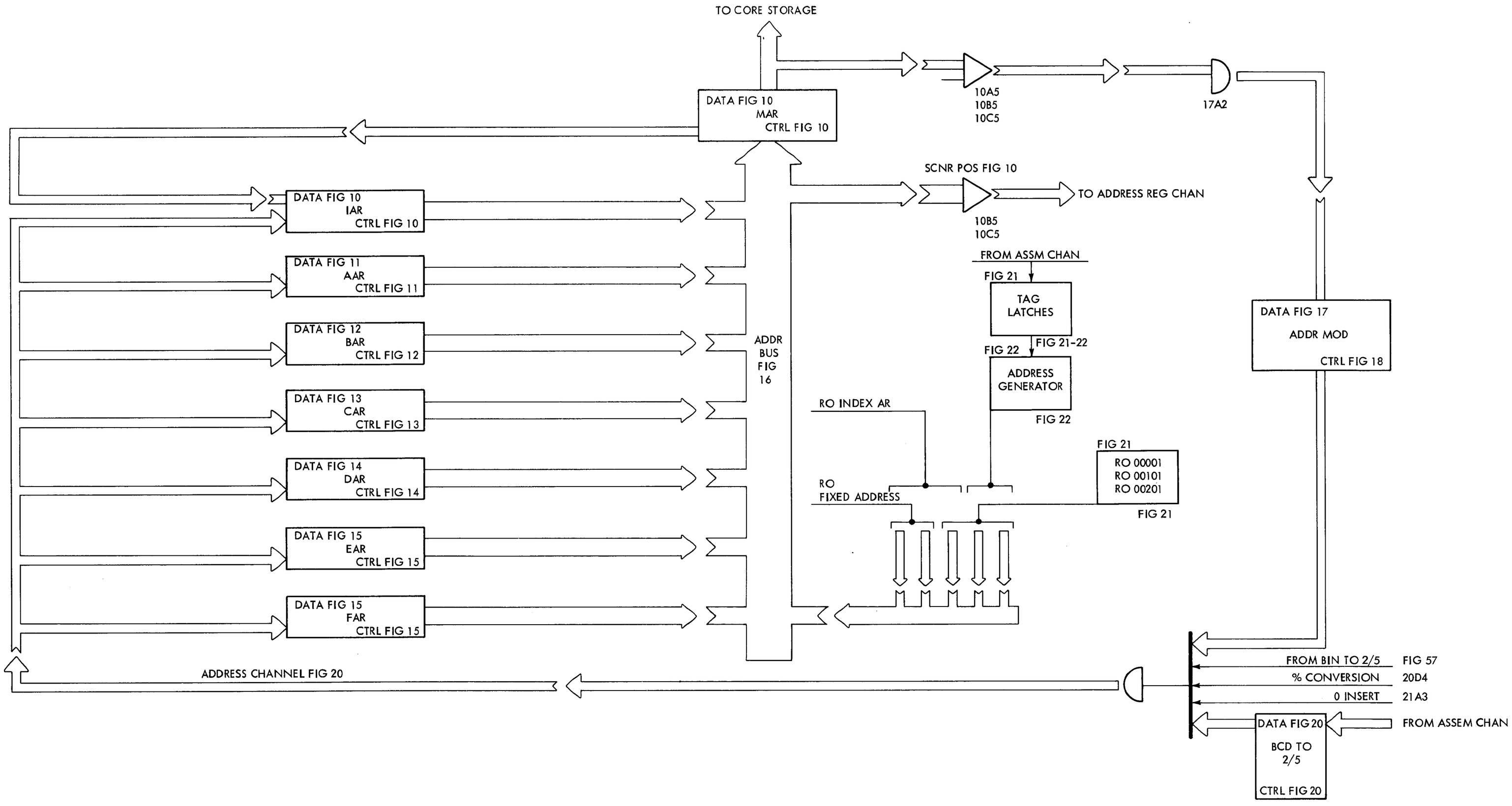
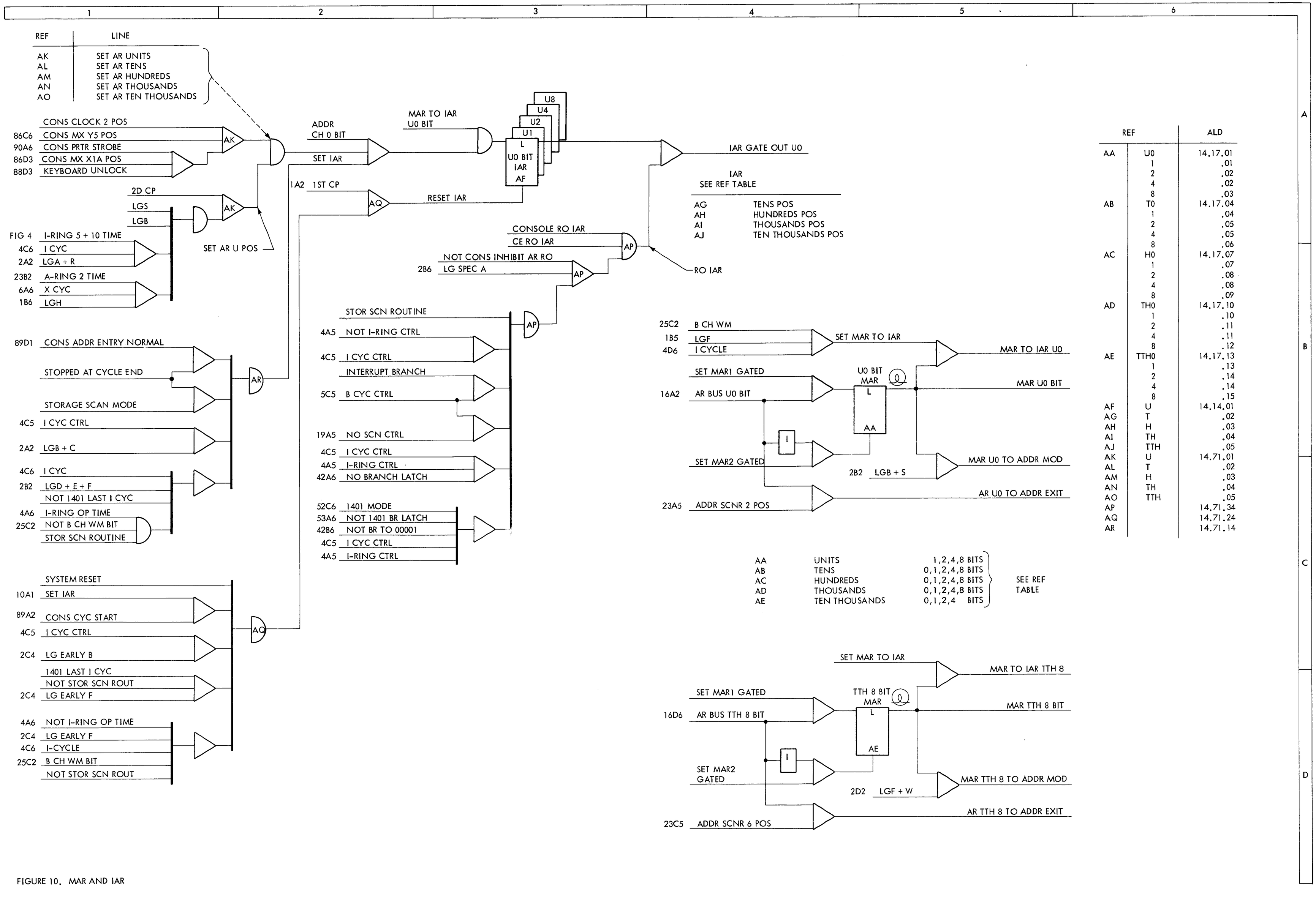


FIGURE 9A. ADDRESSING



REF		ALD
AA	U0	14.17.01
	1	.01
	2	.02
	4	.02
	8	.03
AB	T0	14.17.04
	1	.04
	2	.05
	4	.05
	8	.06
AC	H0	14.17.07
	1	.07
	2	.08
	4	.08
	8	.09
AD	TH0	14.17.10
	1	.10
	2	.11
	4	.11
	8	.12
AE	TTH0	14.17.13
	1	.13
	2	.14
	4	.14
	8	.15
AF	U	14.14.01
AG	T	.02
AH	H	.03
AI	TH	.04
AJ	TTH	.05
AK	U	14.71.01
AL	T	.02
AM	H	.03
AN	TH	.04
AO	TTH	.05
AP		14.71.34
AQ		14.71.24
AR		14.71.14

FIGURE 10. MAR AND IAR

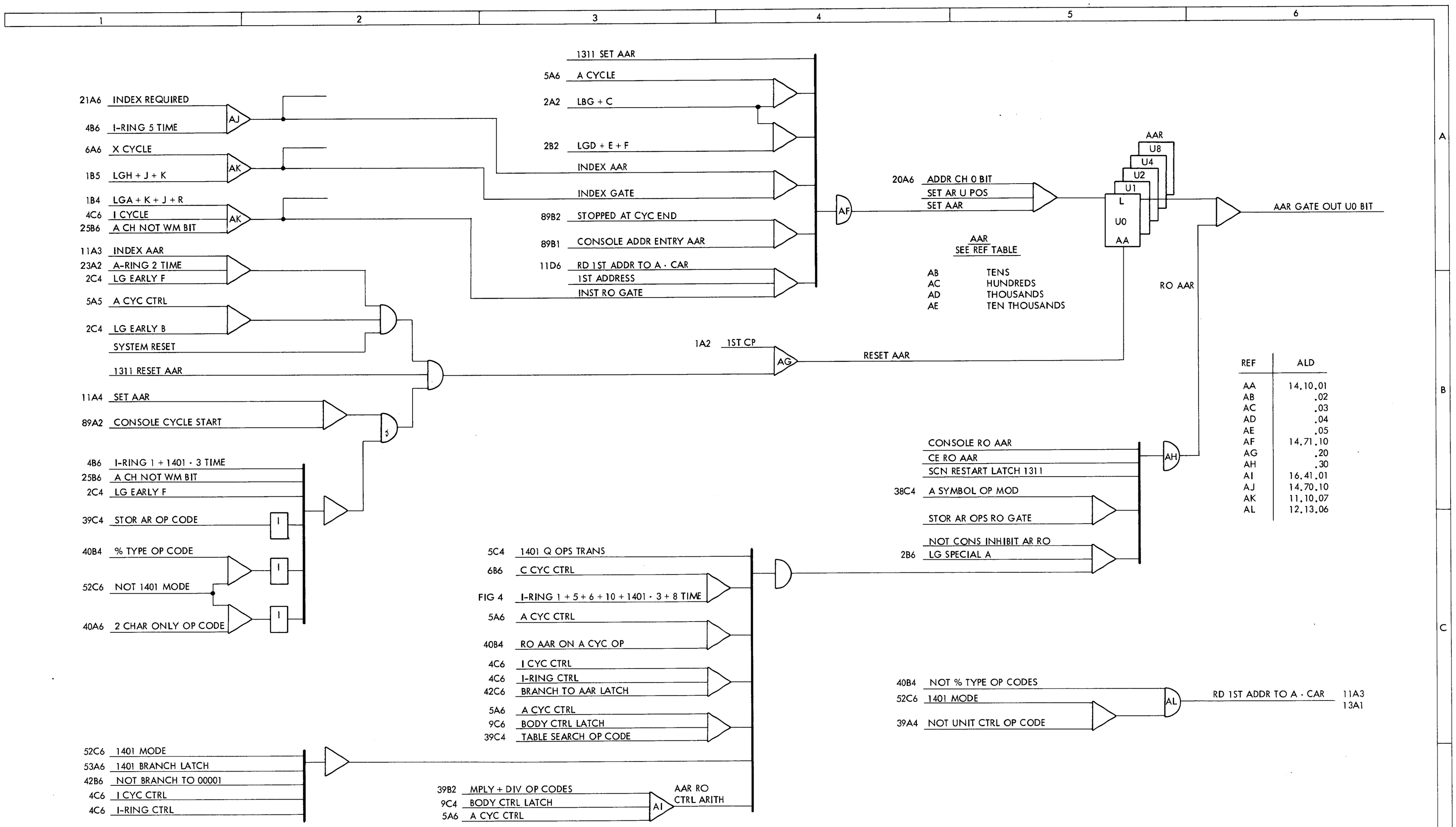


FIGURE 11. AAR

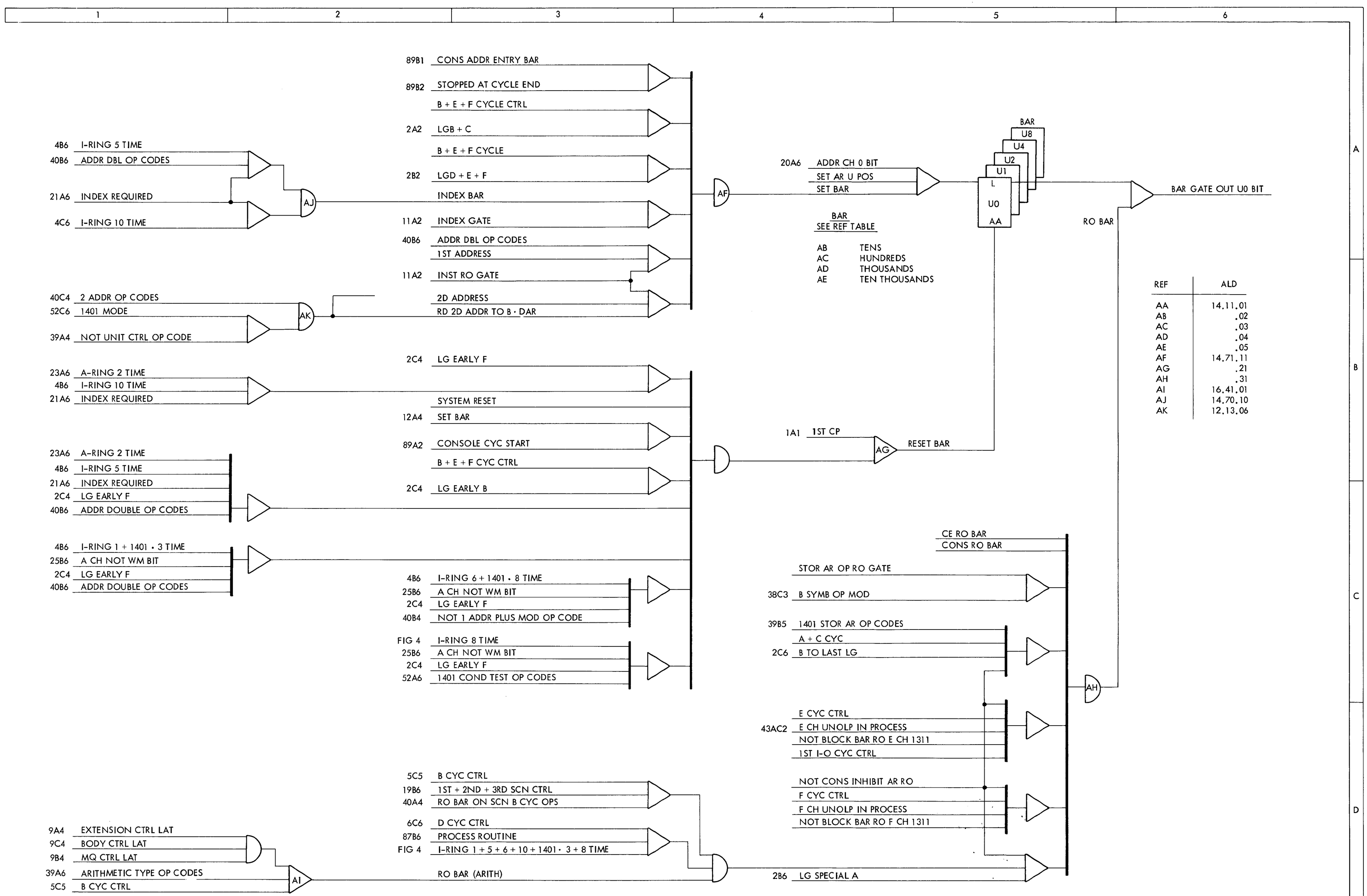


FIGURE 12. BAR

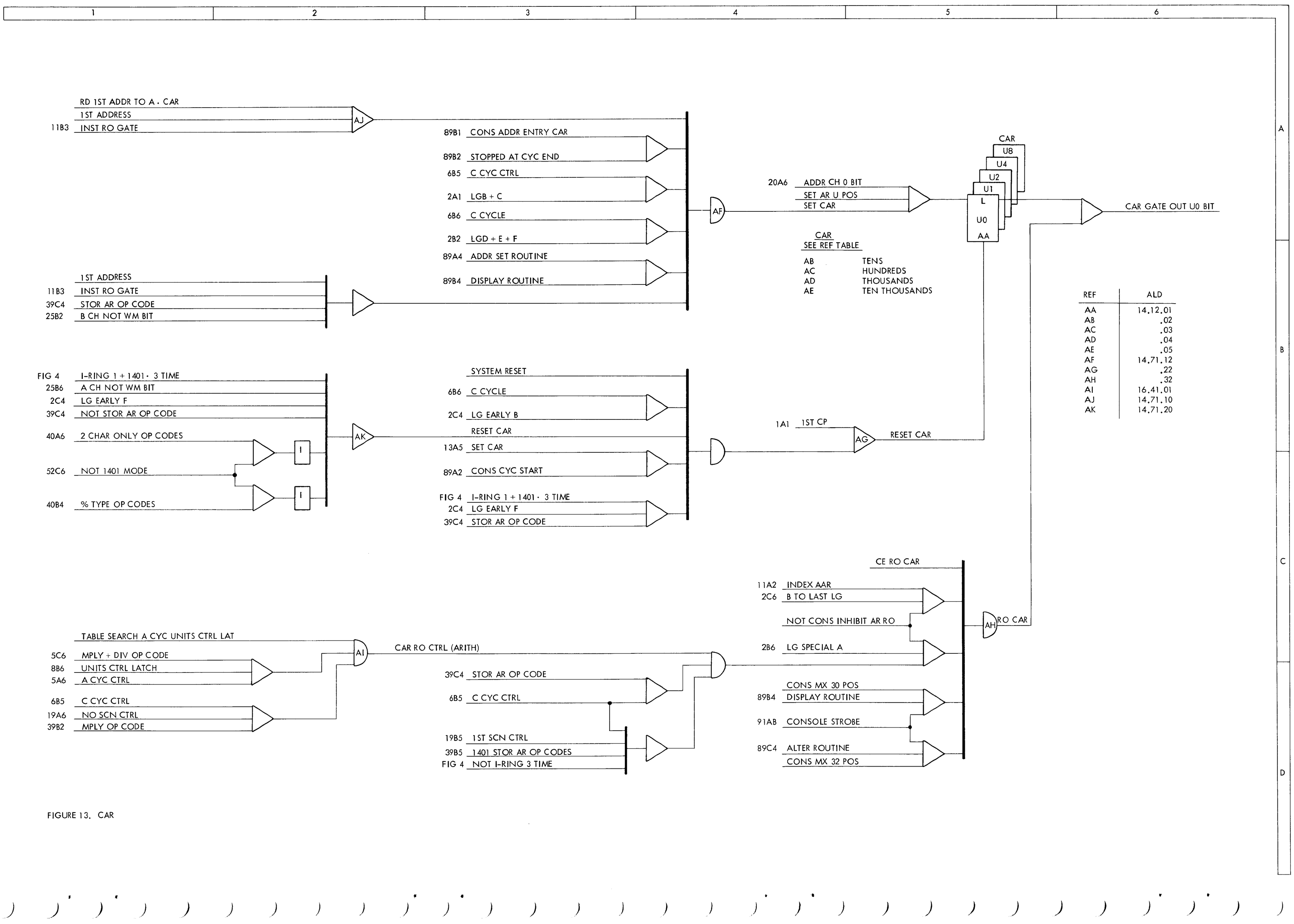


FIGURE 13. CAR

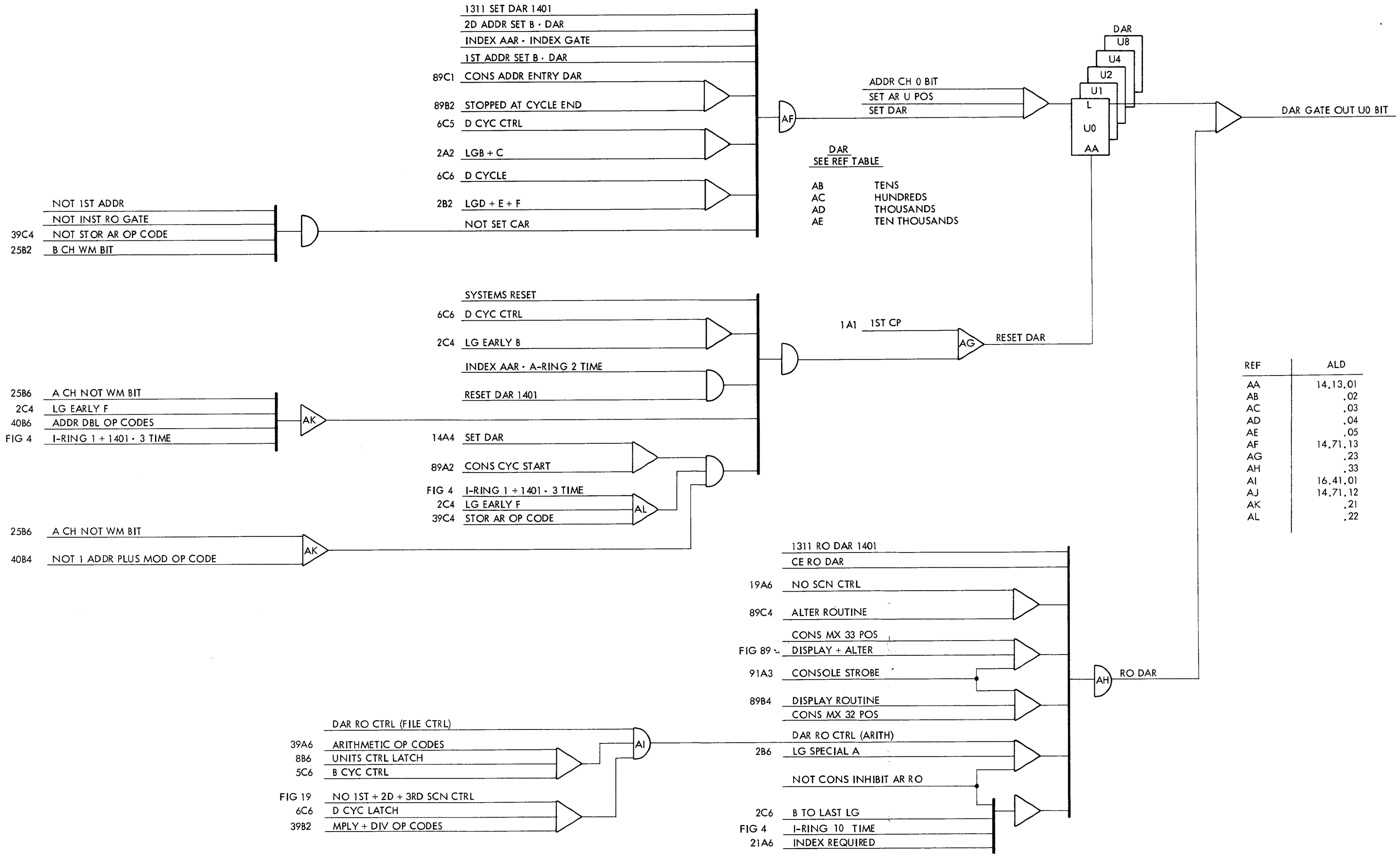


FIGURE 14. DAR

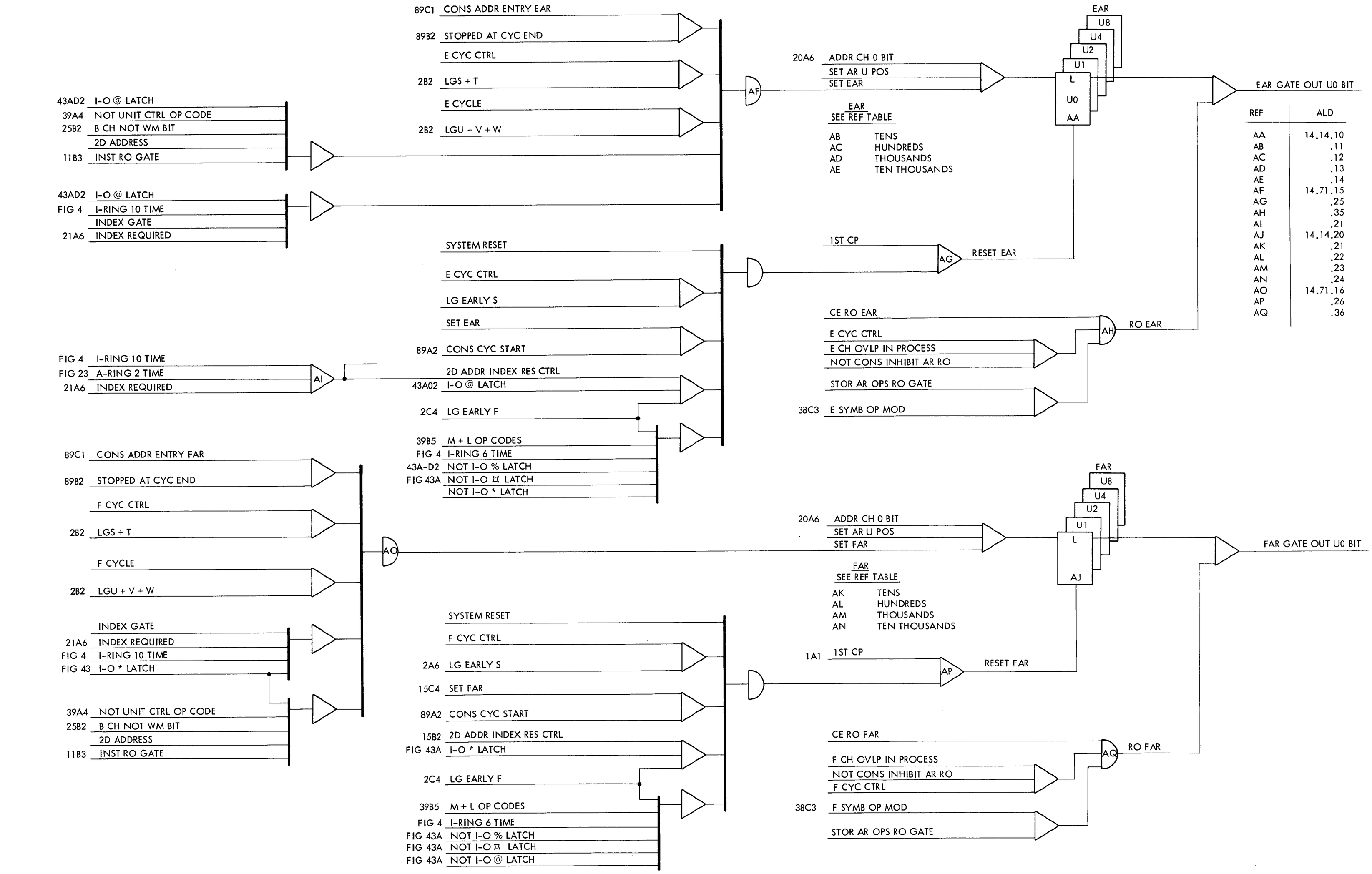


FIGURE 15. EAR AND FAR

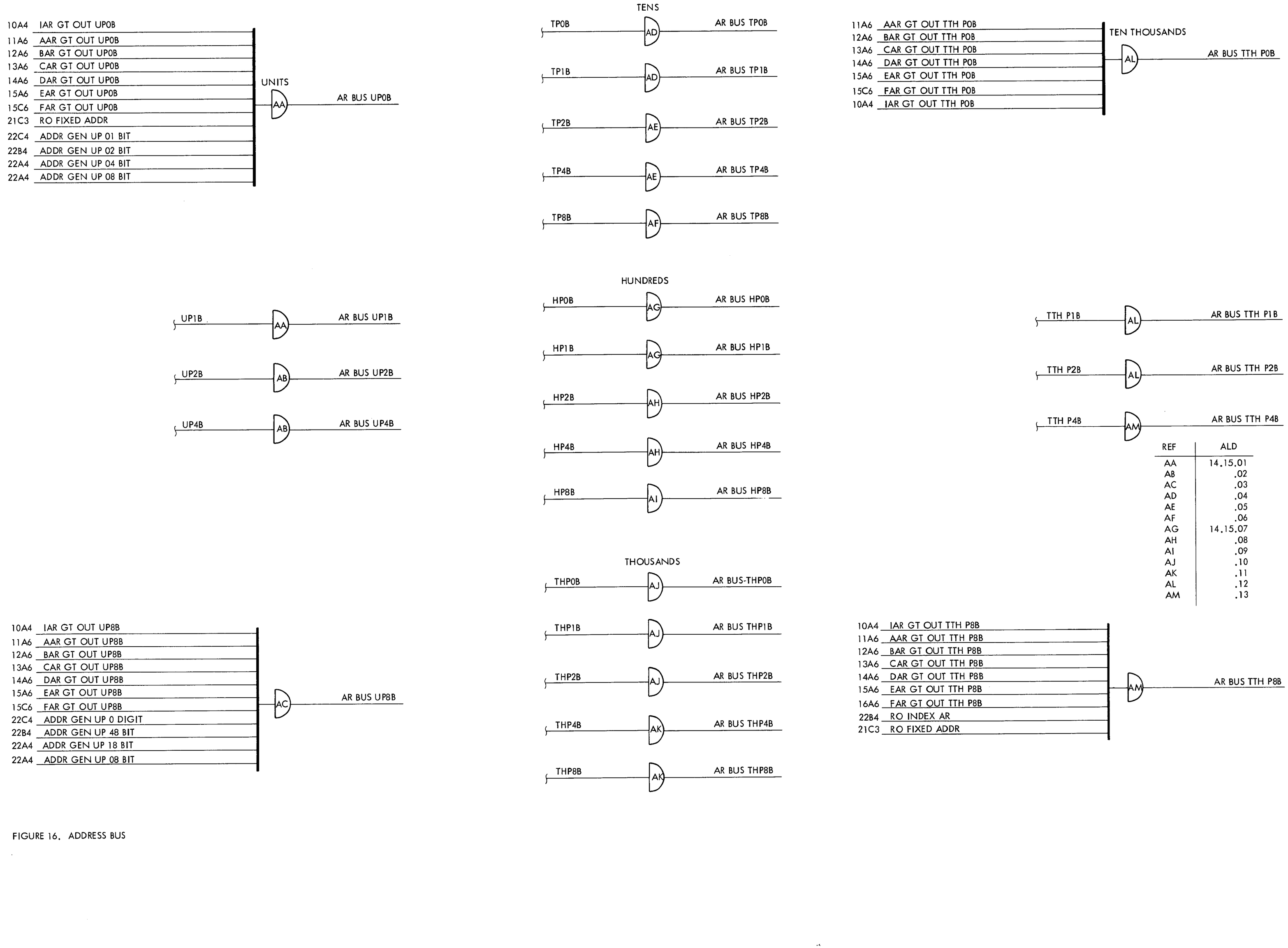


FIGURE 16. ADDRESS BUS

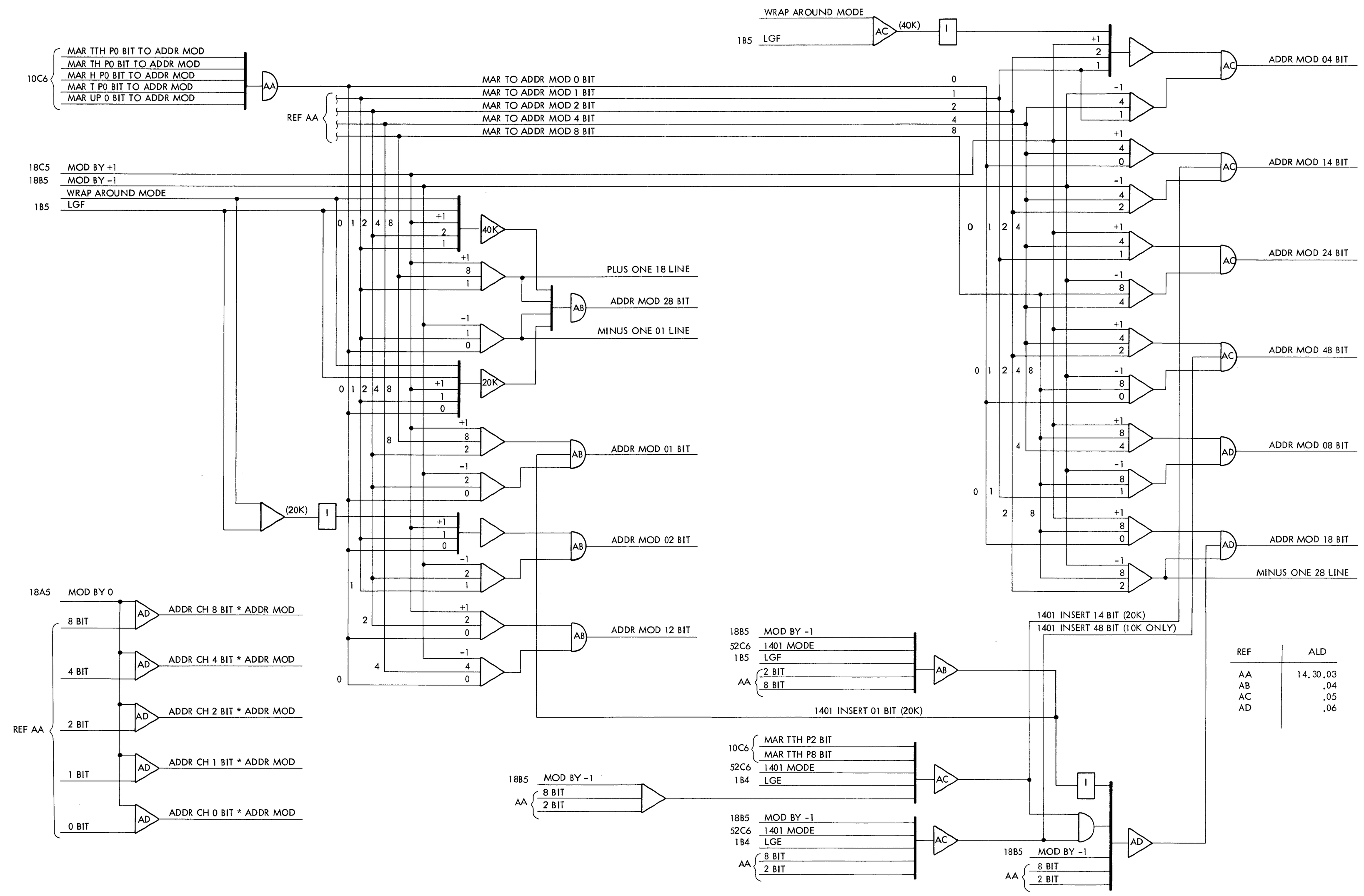
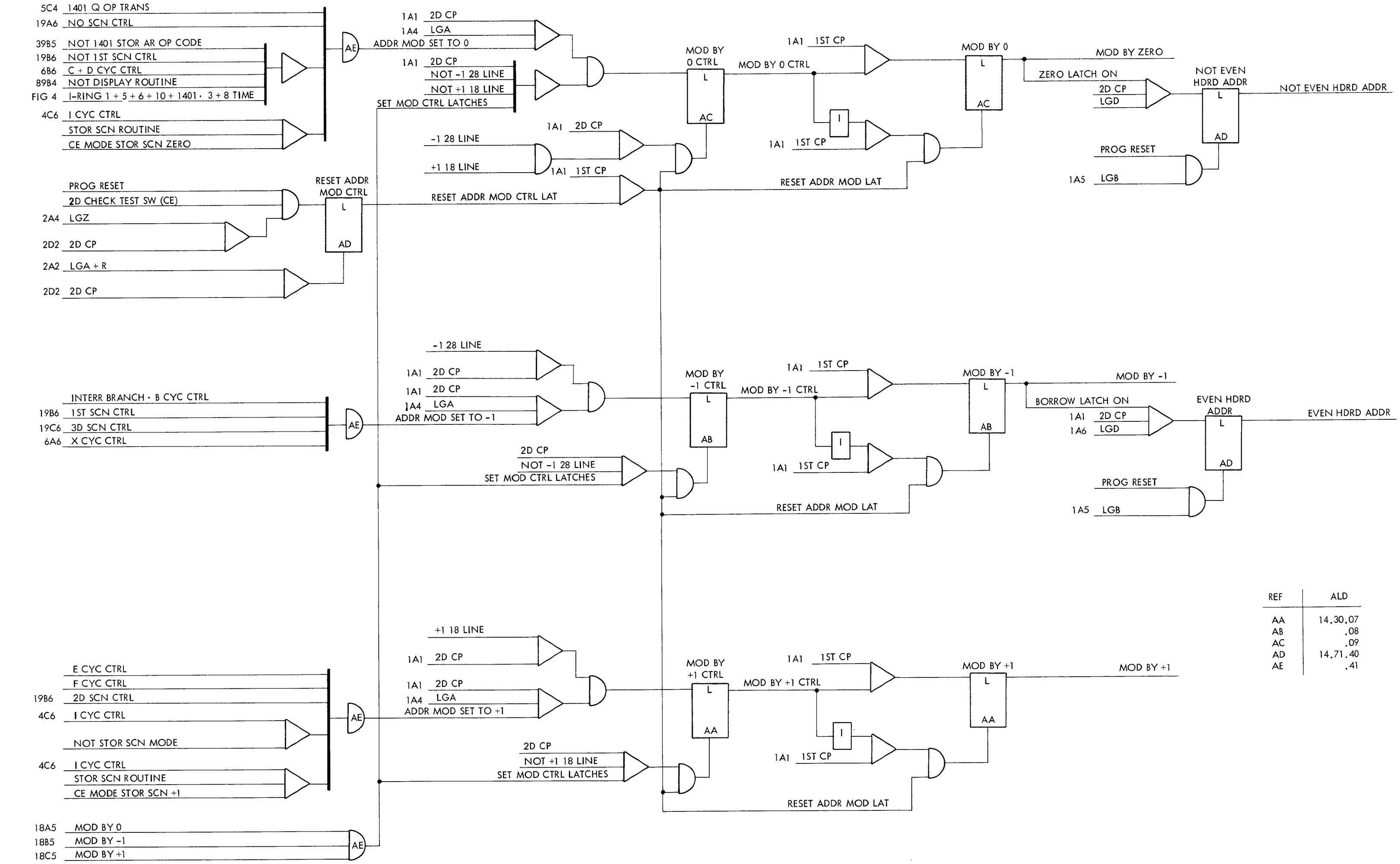


FIGURE 17. ADDR MOD



REF	ALD
AA	14.30.07
AB	.08
AC	.09
AD	14.71.40
AE	.41

FIGURE 18. ADDRESS MOD CONTROL

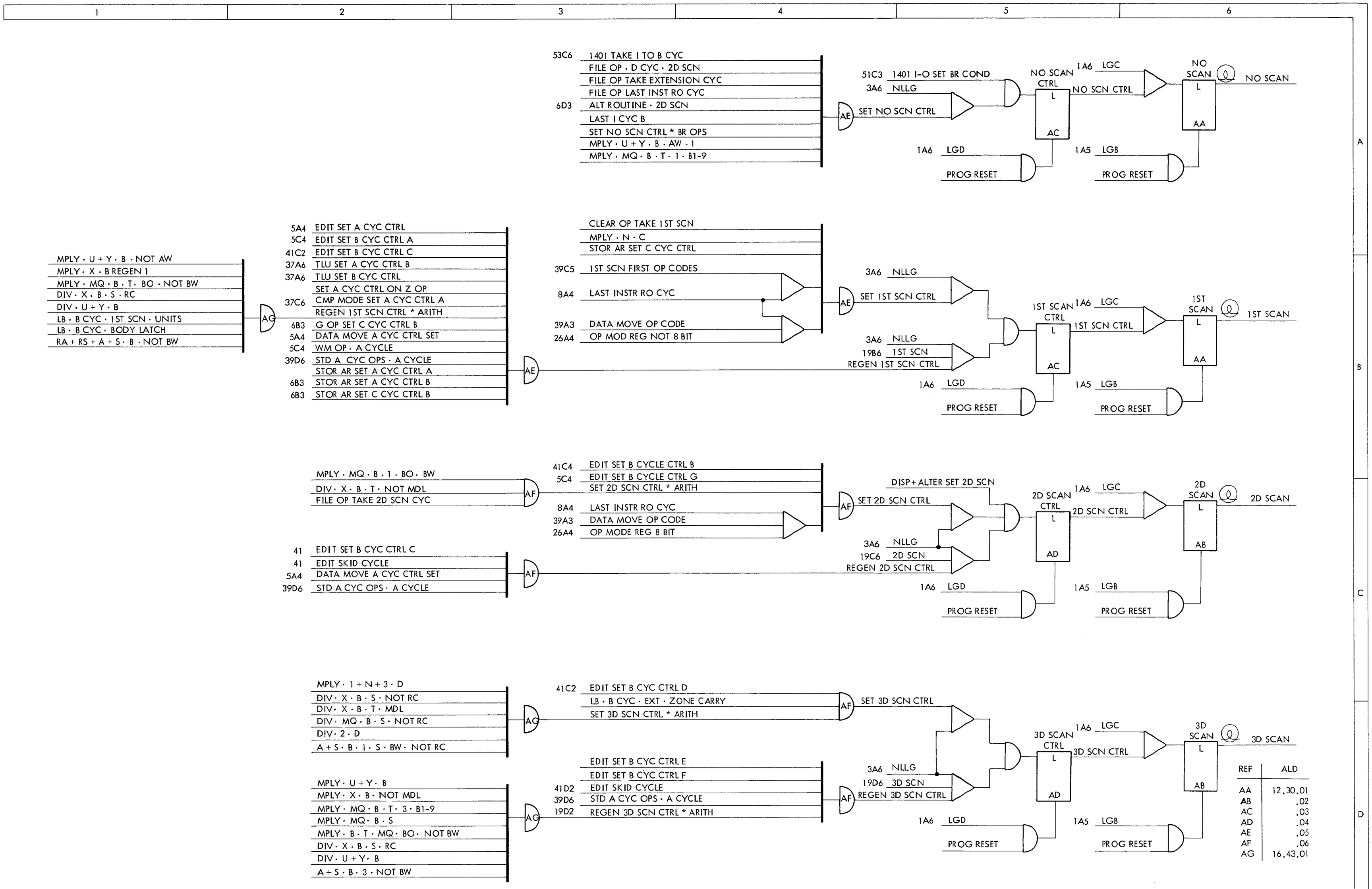
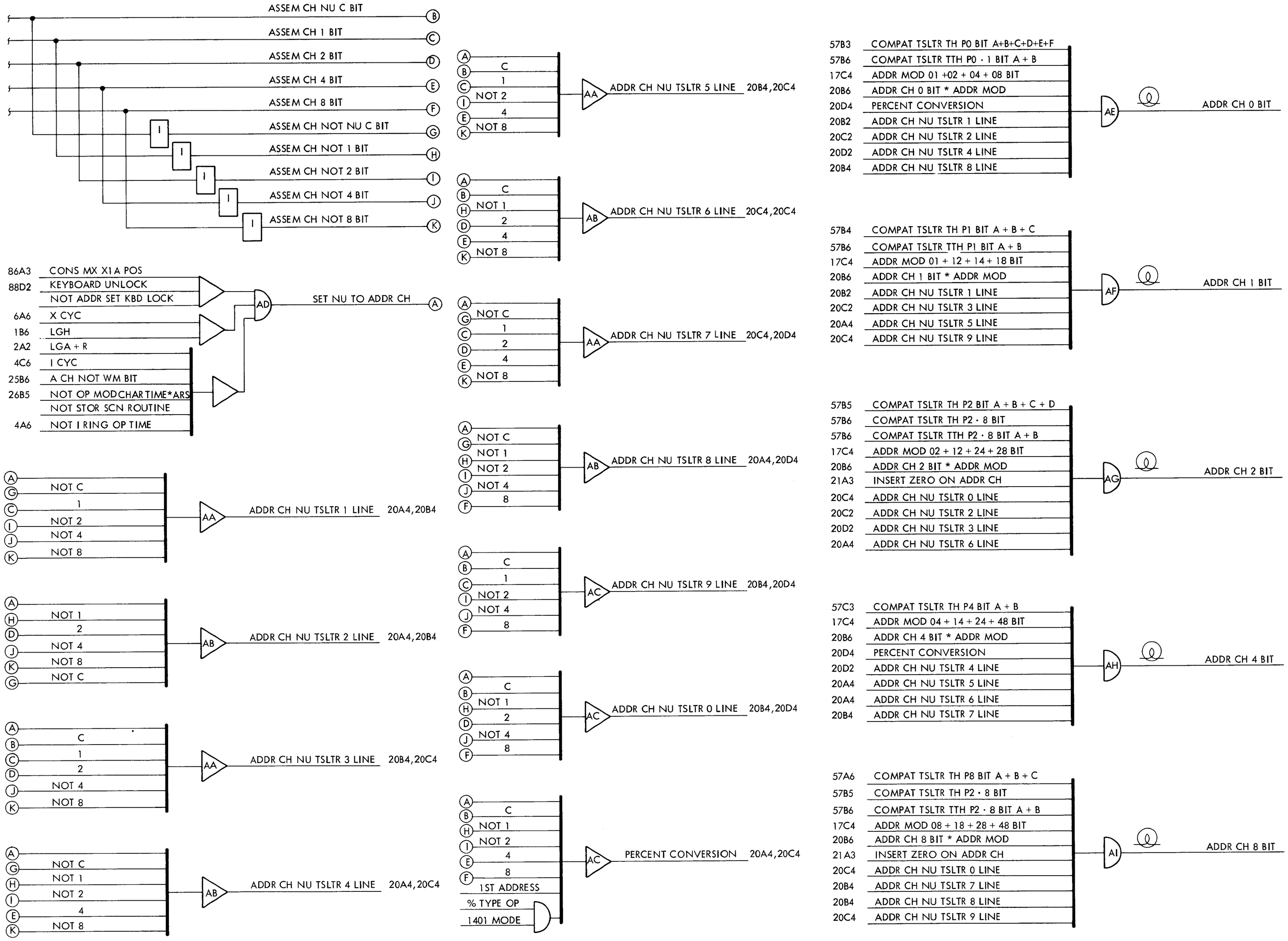
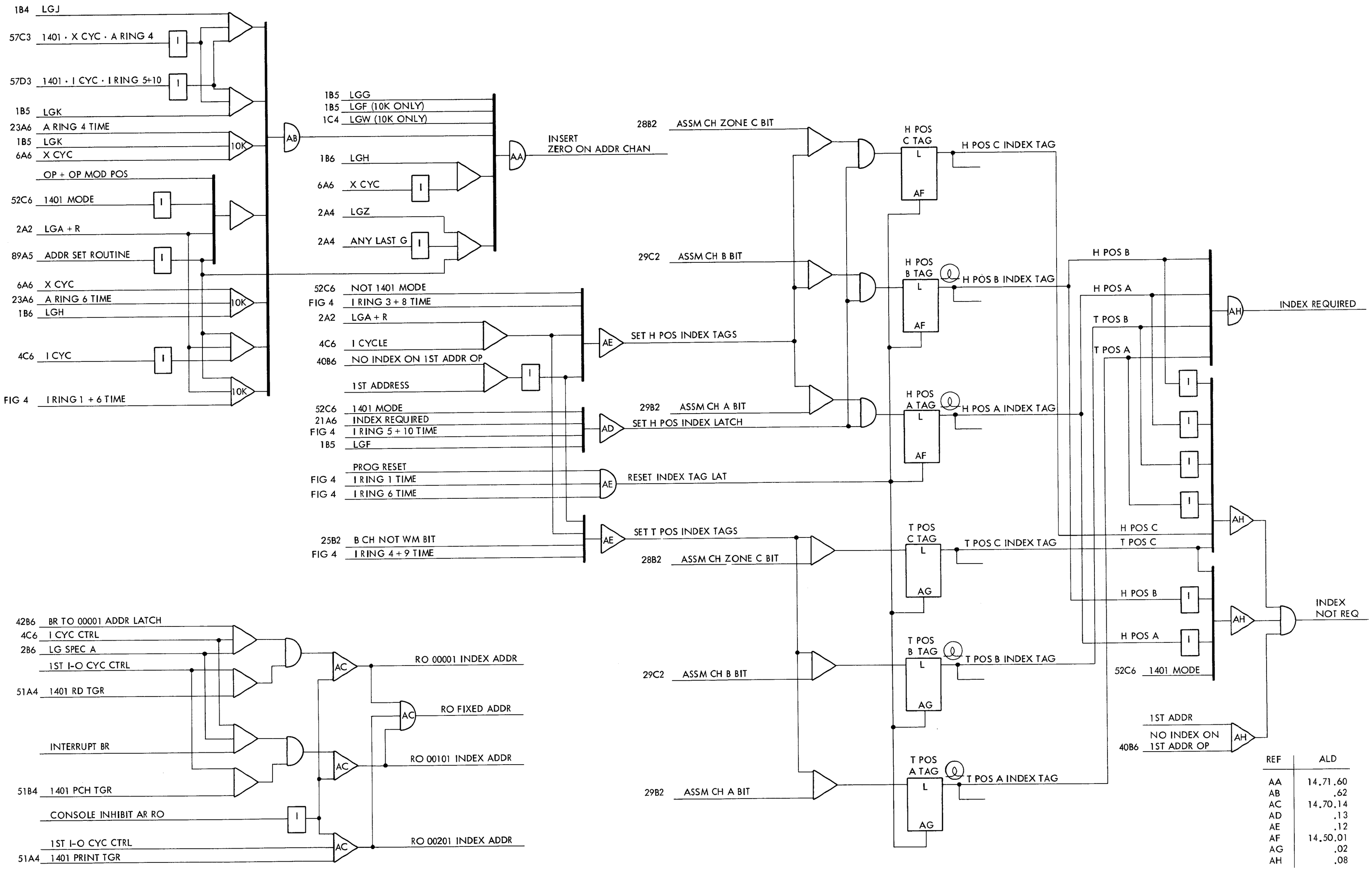


FIGURE 19. SCAN LATCHES AND CTRLS



REF	ALD
AA	14.42.03
AB	.04
AC	.05
AD	14.71.61
AE	14.45.01
AF	.02
AG	.03
AH	.04
AI	.05

FIGURE 20. BCD TO 2/5 AND ADDR CH



REF	ALD
AA	14.71.60
AB	.62
AC	14.70.14
AD	.13
AE	.12
AF	14.50.01
AG	.02
AH	.08

FIGURE 21. SPECIAL AND INDEX ADDRESSING

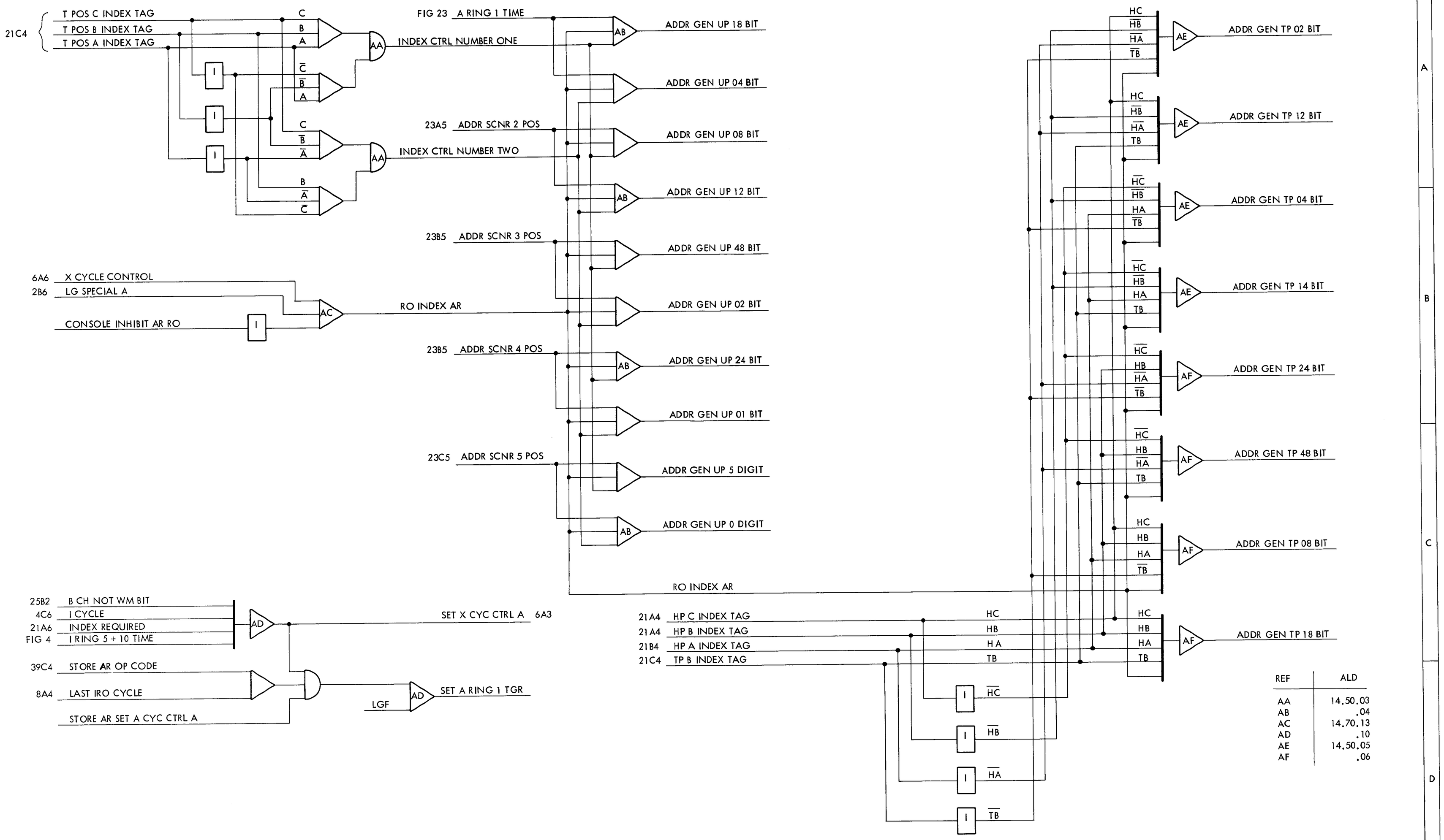
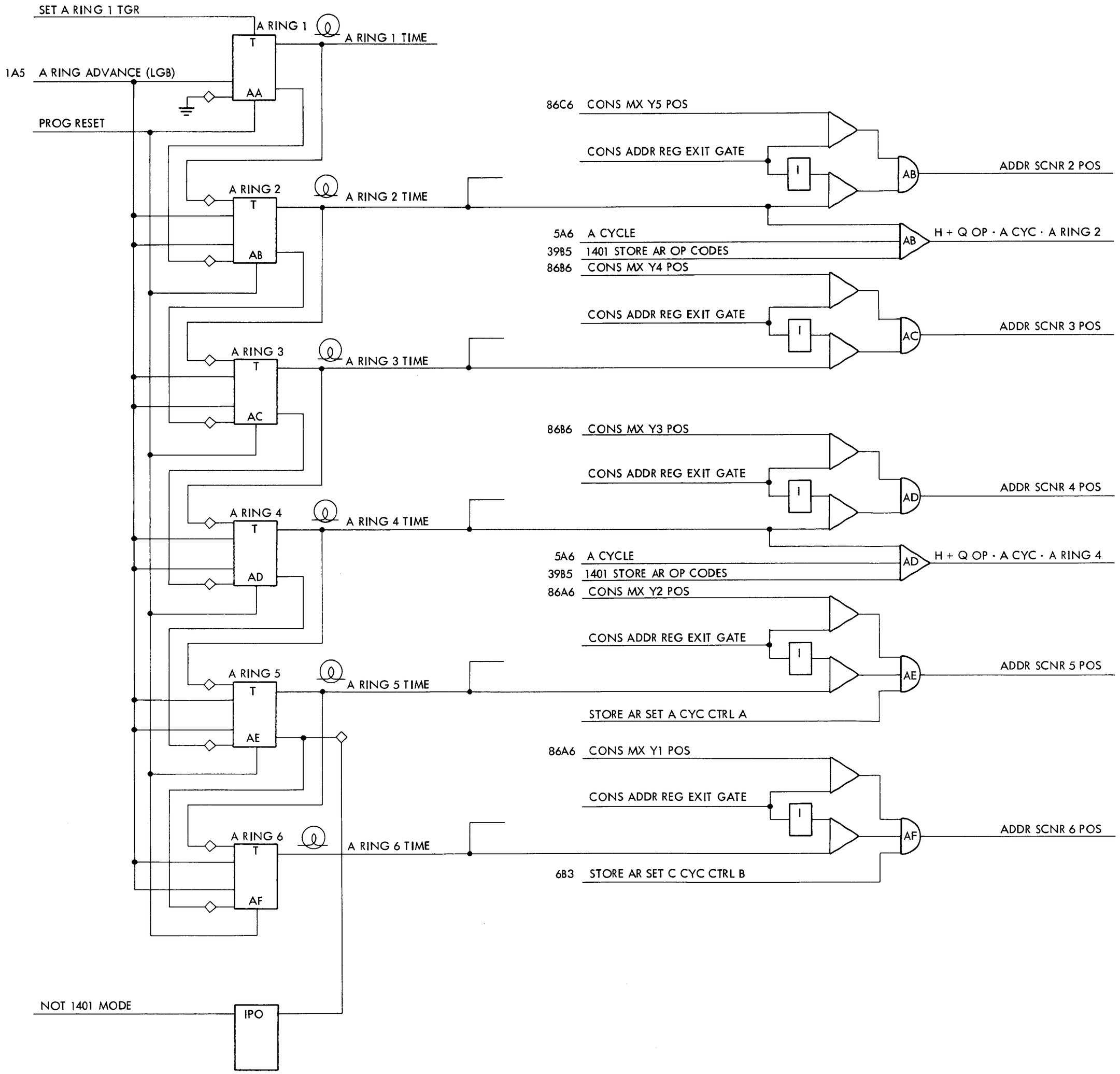


FIGURE 22. ADDRESS GENERATOR AND INDEX CONTROL



REF	ALD
AA	14.70.01
AB	.02
AC	.03
AD	.04
AE	.05
AF	.06
AG	.07

FIGURE 23. A RING AND ADDRESS SCNR

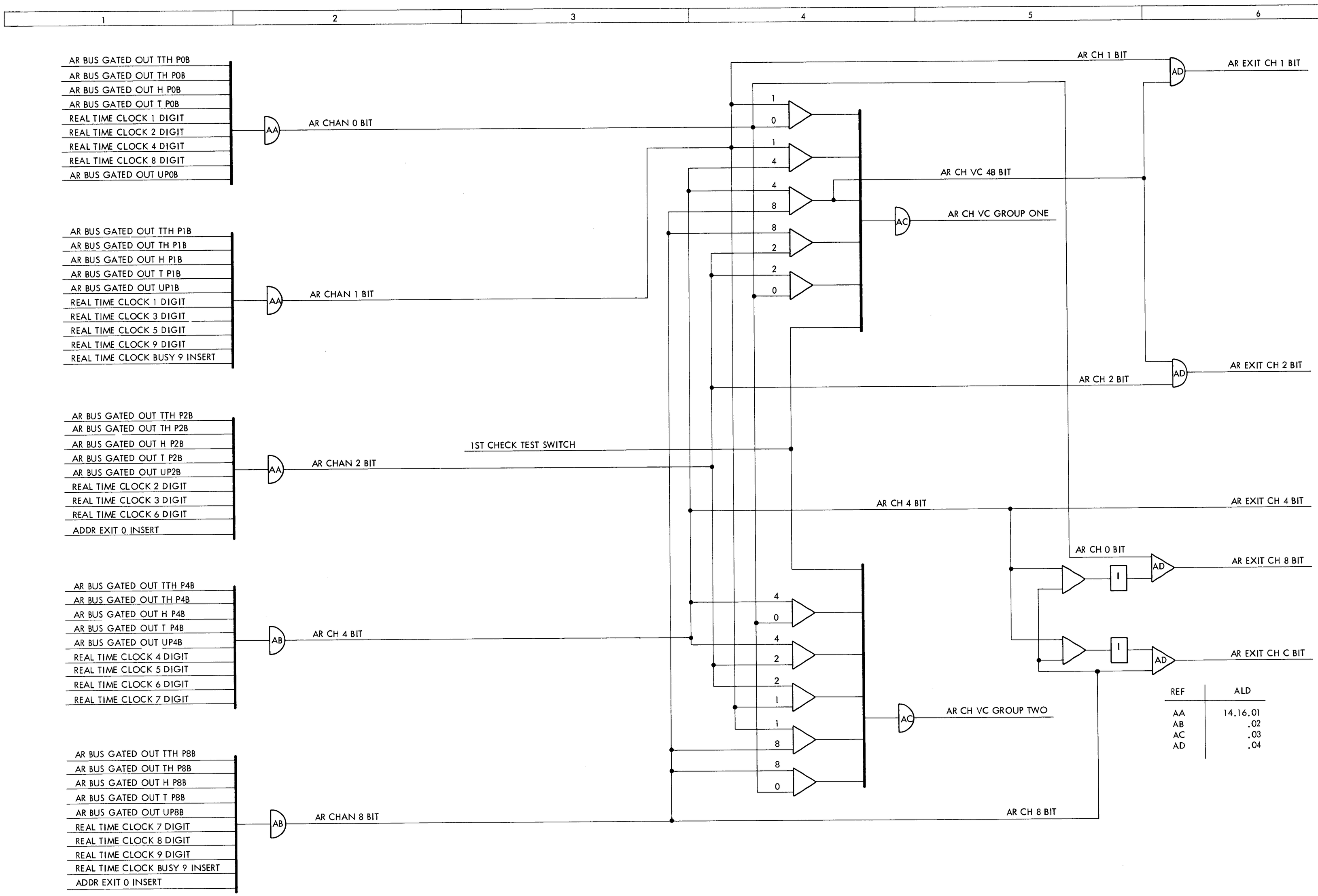


FIGURE 24. ADDR REG AND ADDR EXIT CHAN, 2/5 - BCD

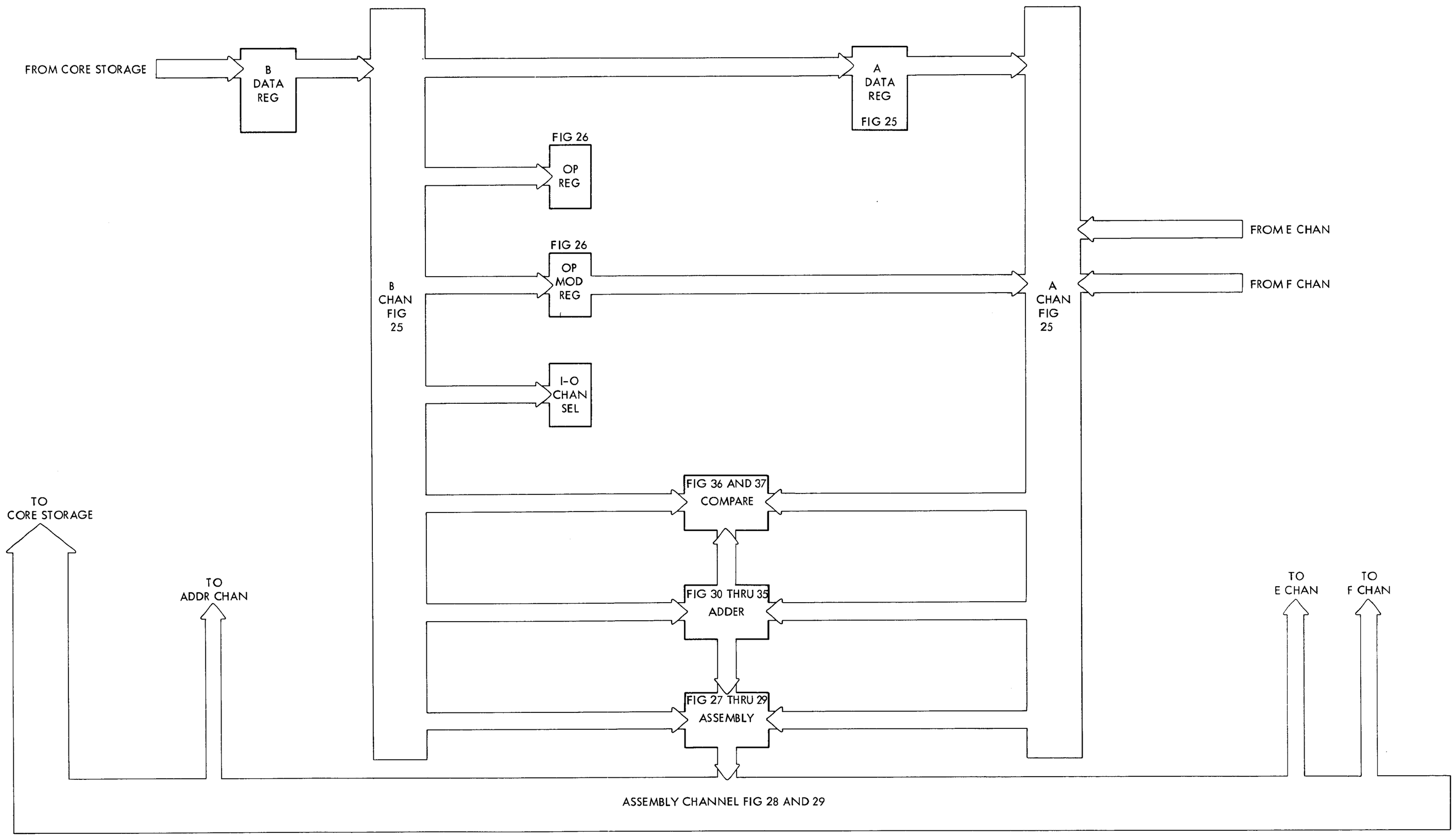


FIGURE 24A. A AND B CHANNEL

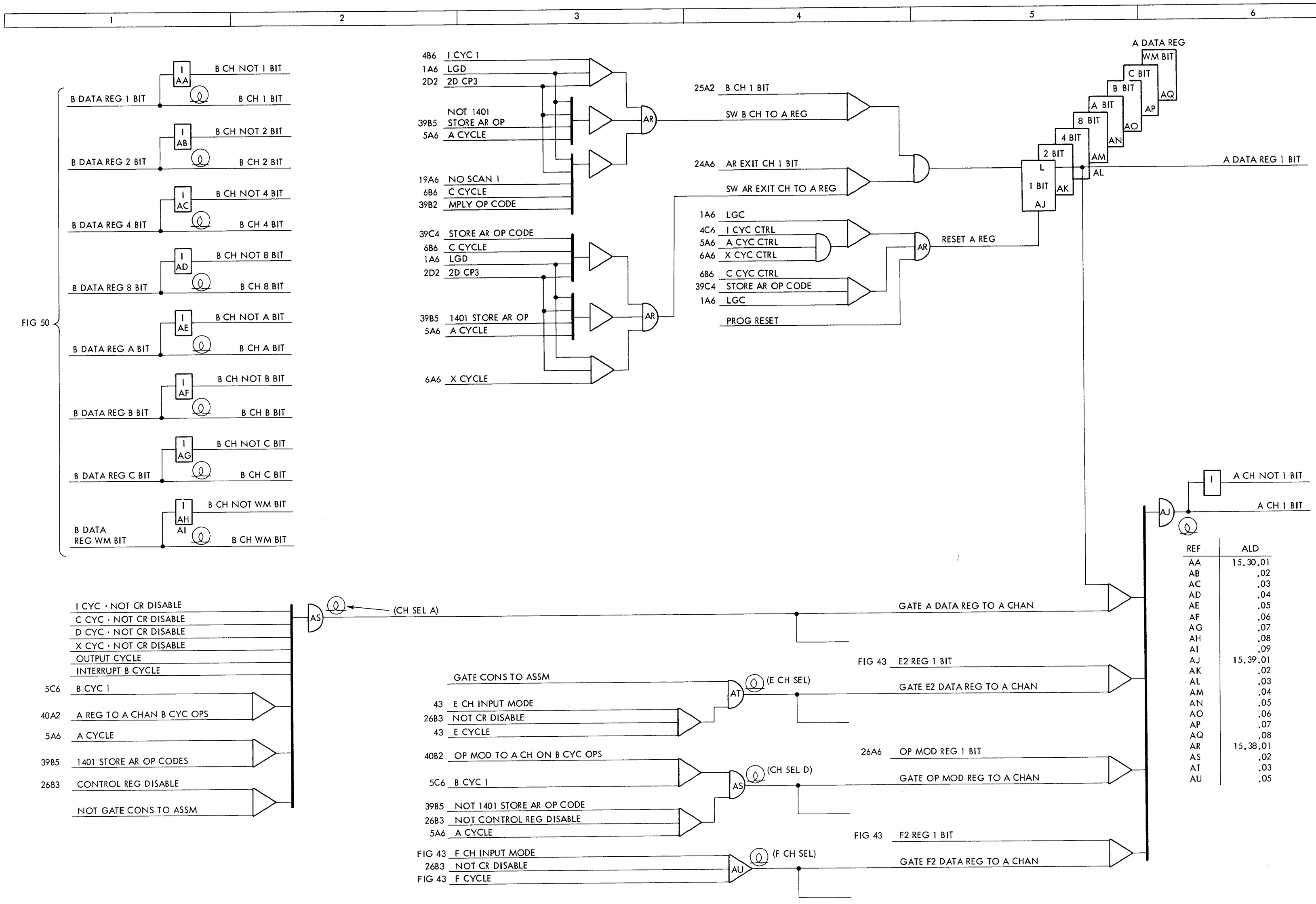


FIGURE 25. A AND B CHAN, AND A DATA REGISTER

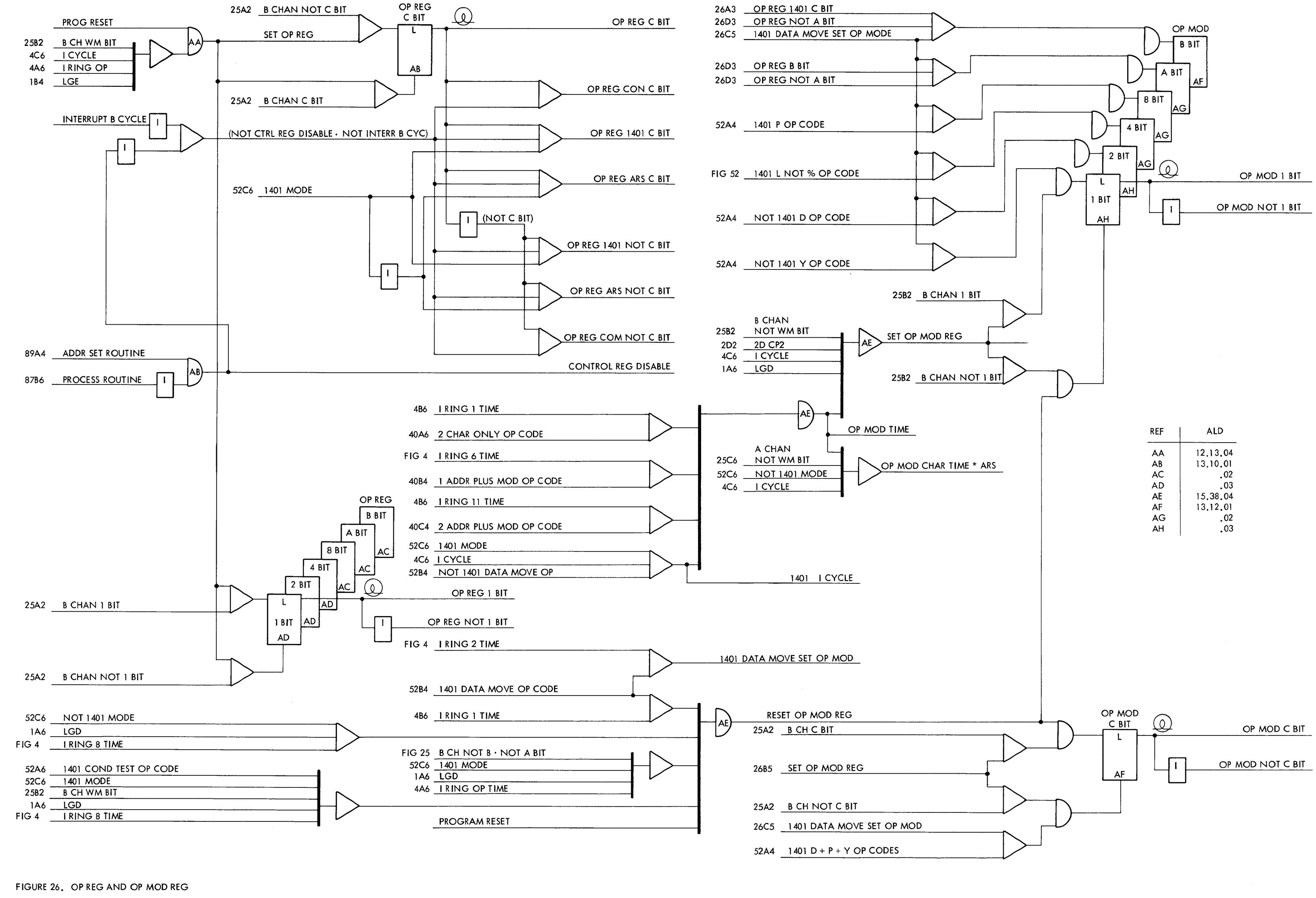


FIGURE 26. OP REG AND OP MOD REG

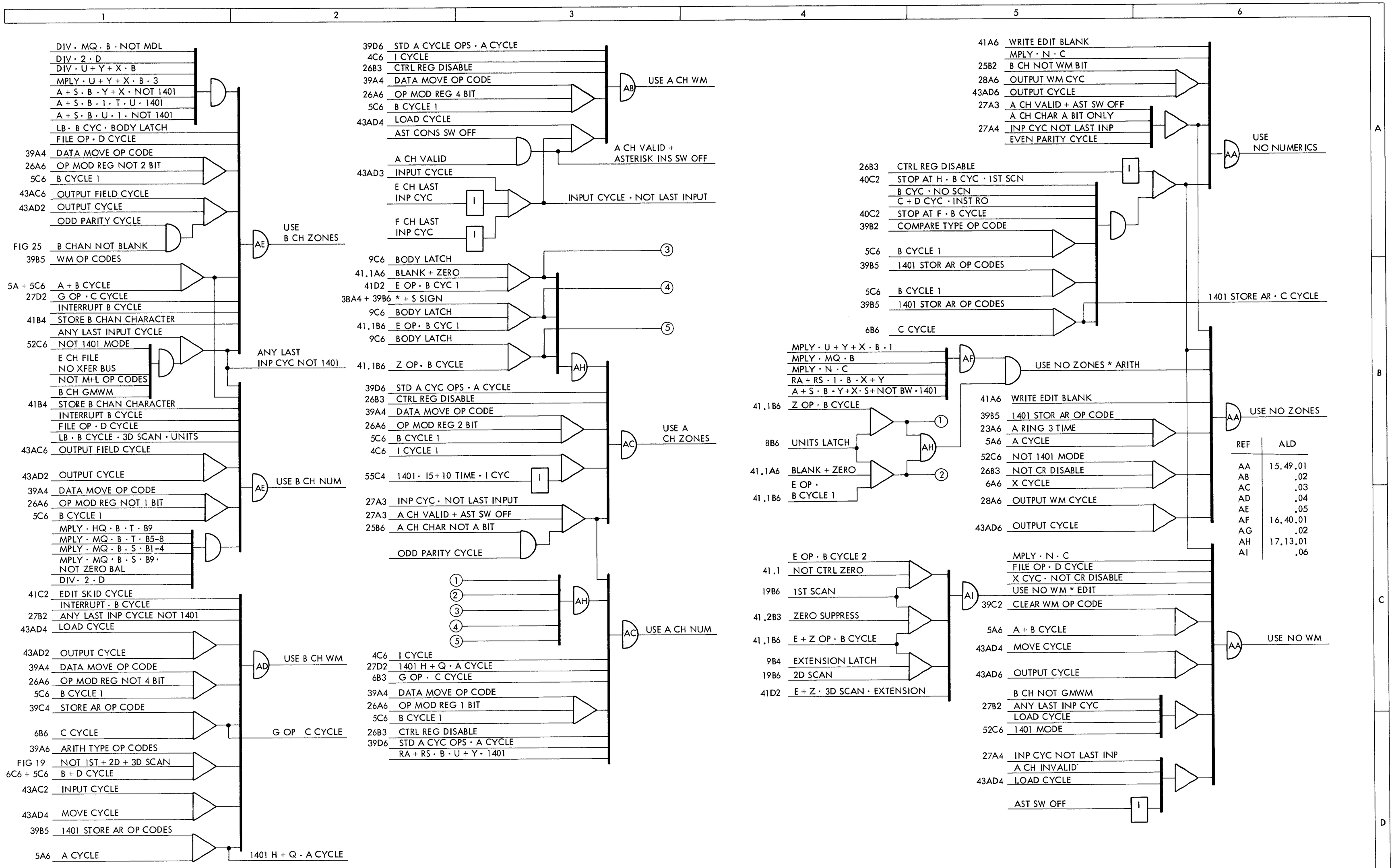
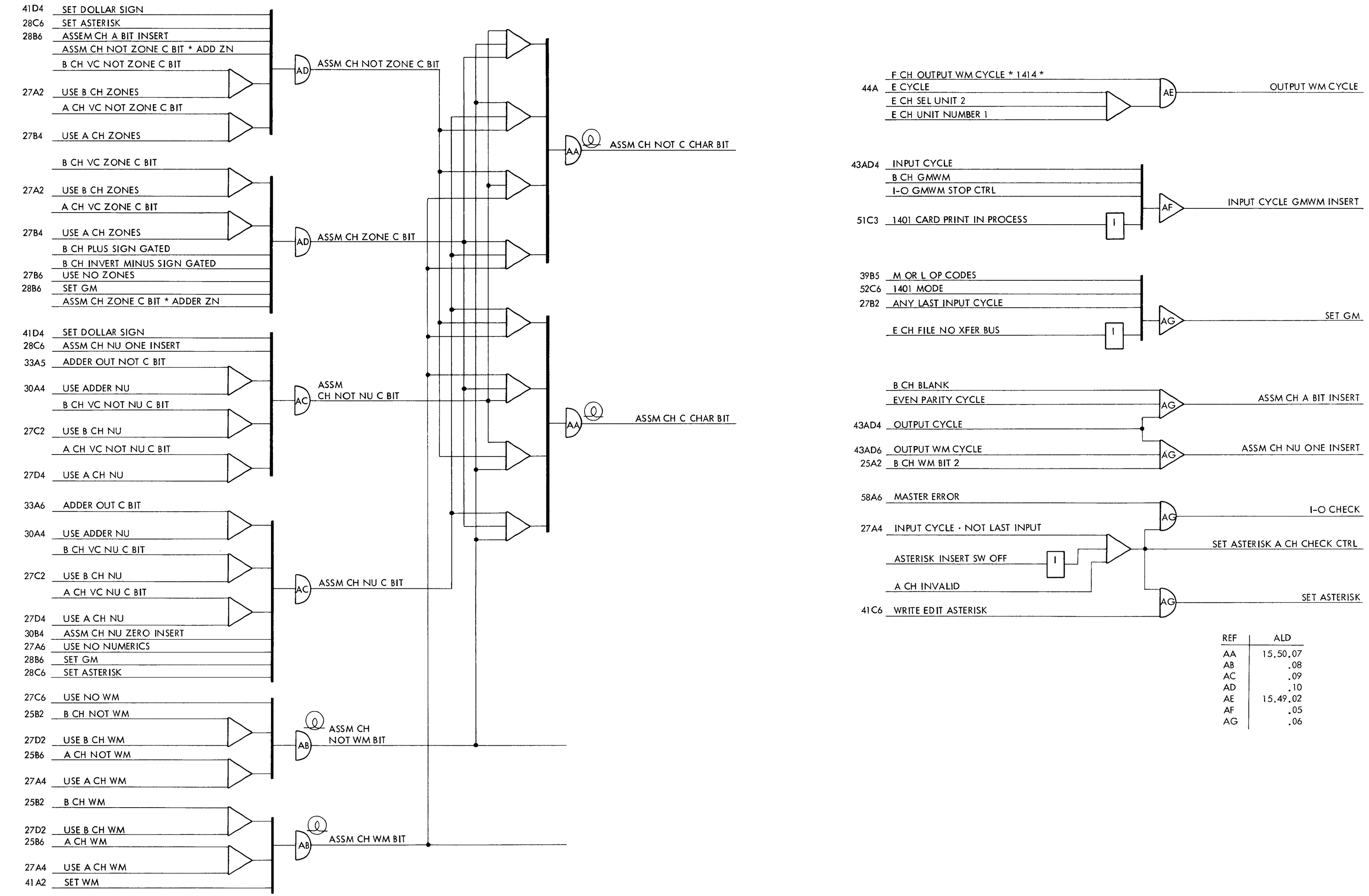
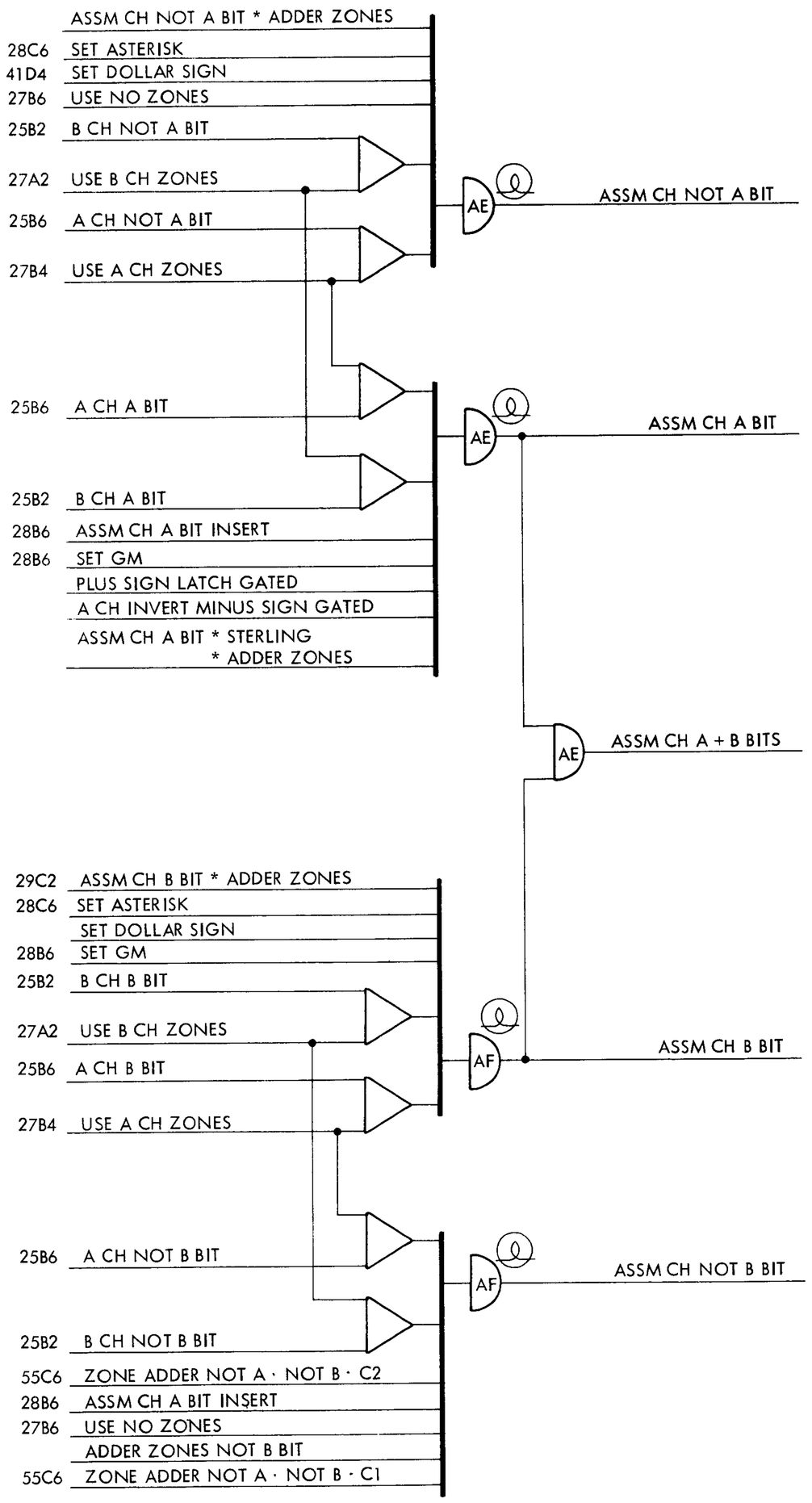


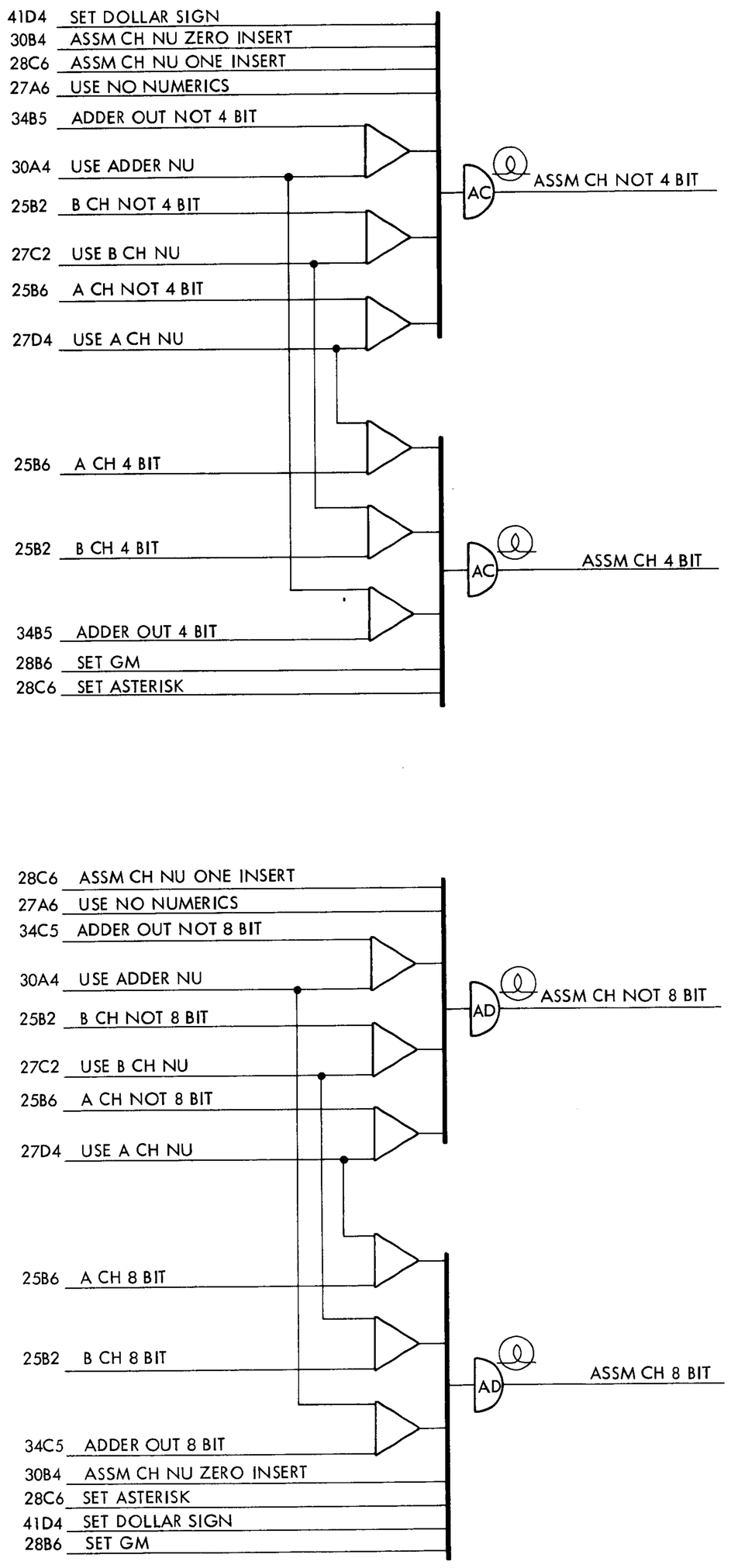
FIGURE 27. ASSEMBLY CONTROLS

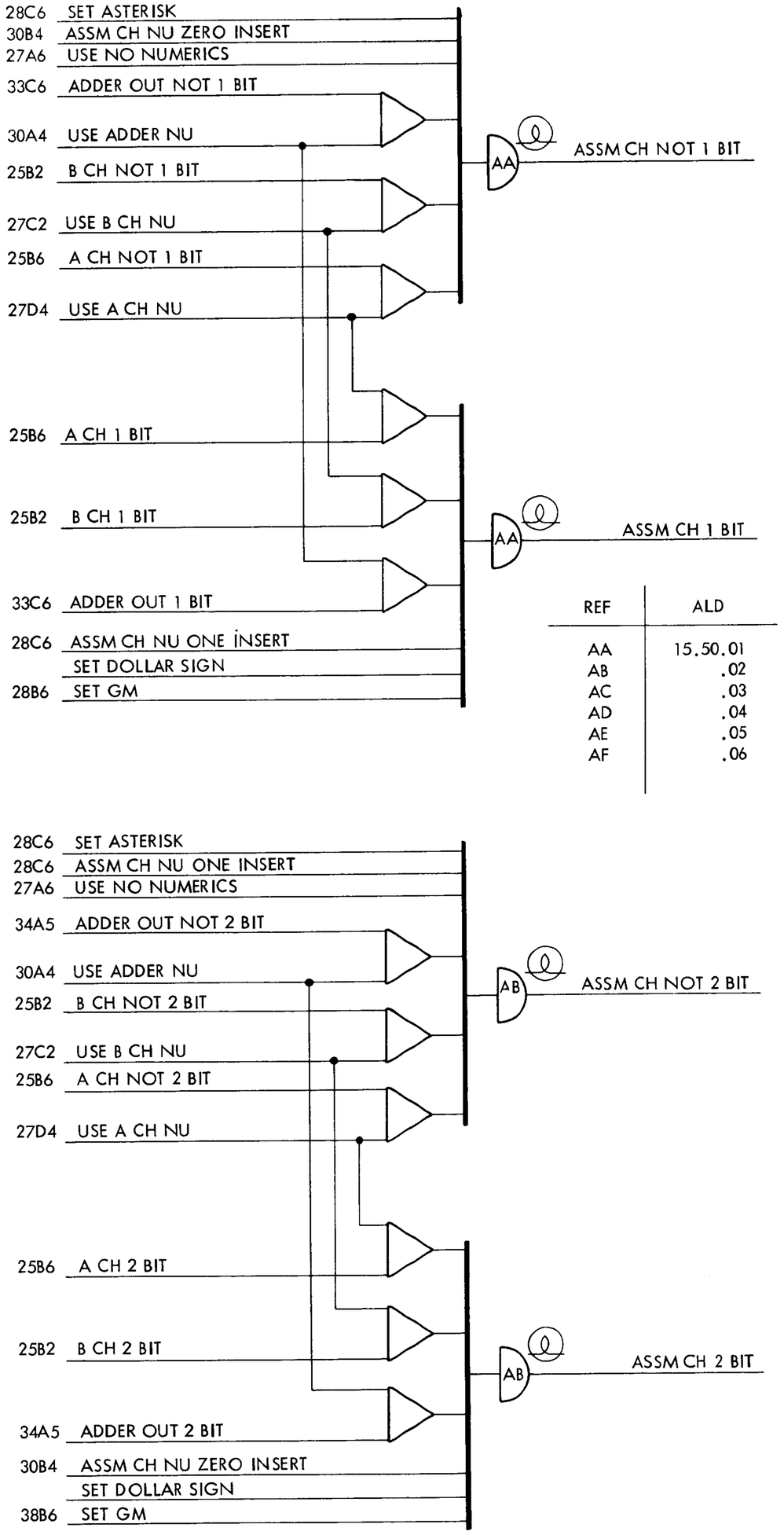


REF	ALD
AA	15.50.07
AB	.08
AC	.09
AD	.10
AE	15.49.02
AF	.05
AG	.06

FIGURE 28. ASSEMBLY CHAN C AND WM BIT

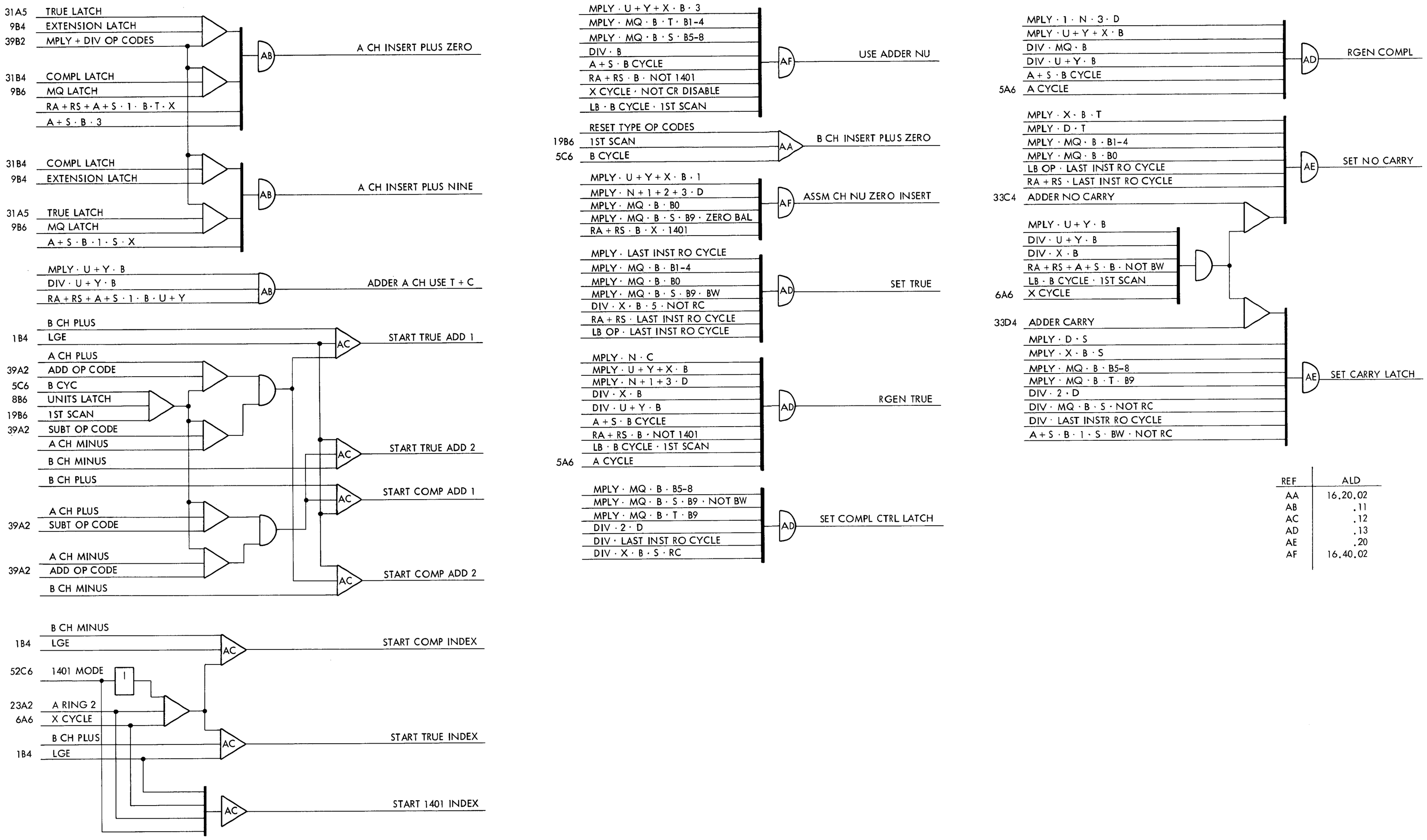






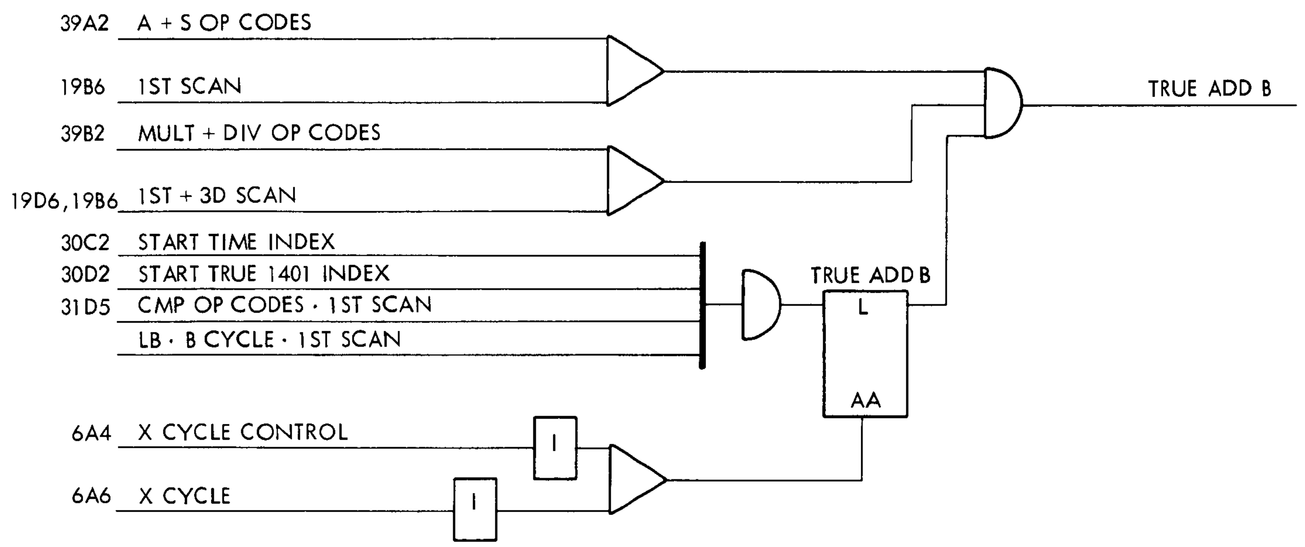
REF	ALD
AA	15.50.01
AB	.02
AC	.03
AD	.04
AE	.05
AF	.06

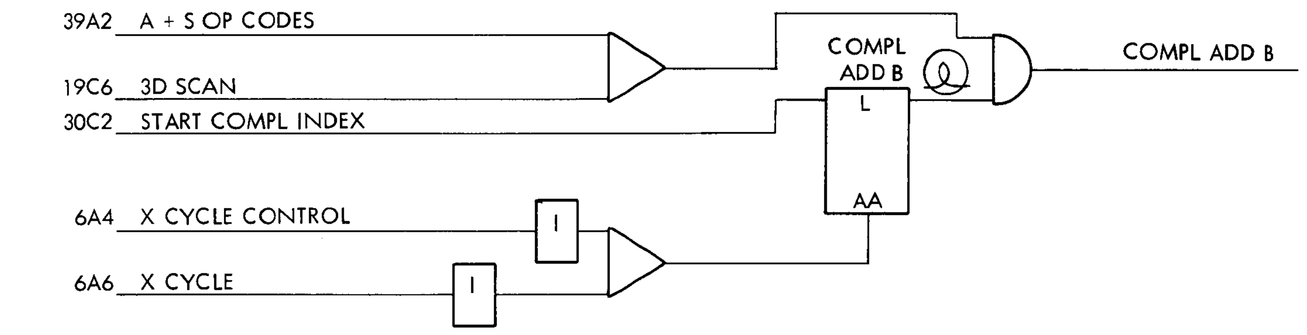
FIGURE 29. ASSM CHAN 1,2,4,8,A AND B BITS



REF	ALD
AA	16.20.02
AB	.11
AC	.12
AD	.13
AE	.20
AF	16.40.02

FIGURE 30. ADDER CTRL LINES





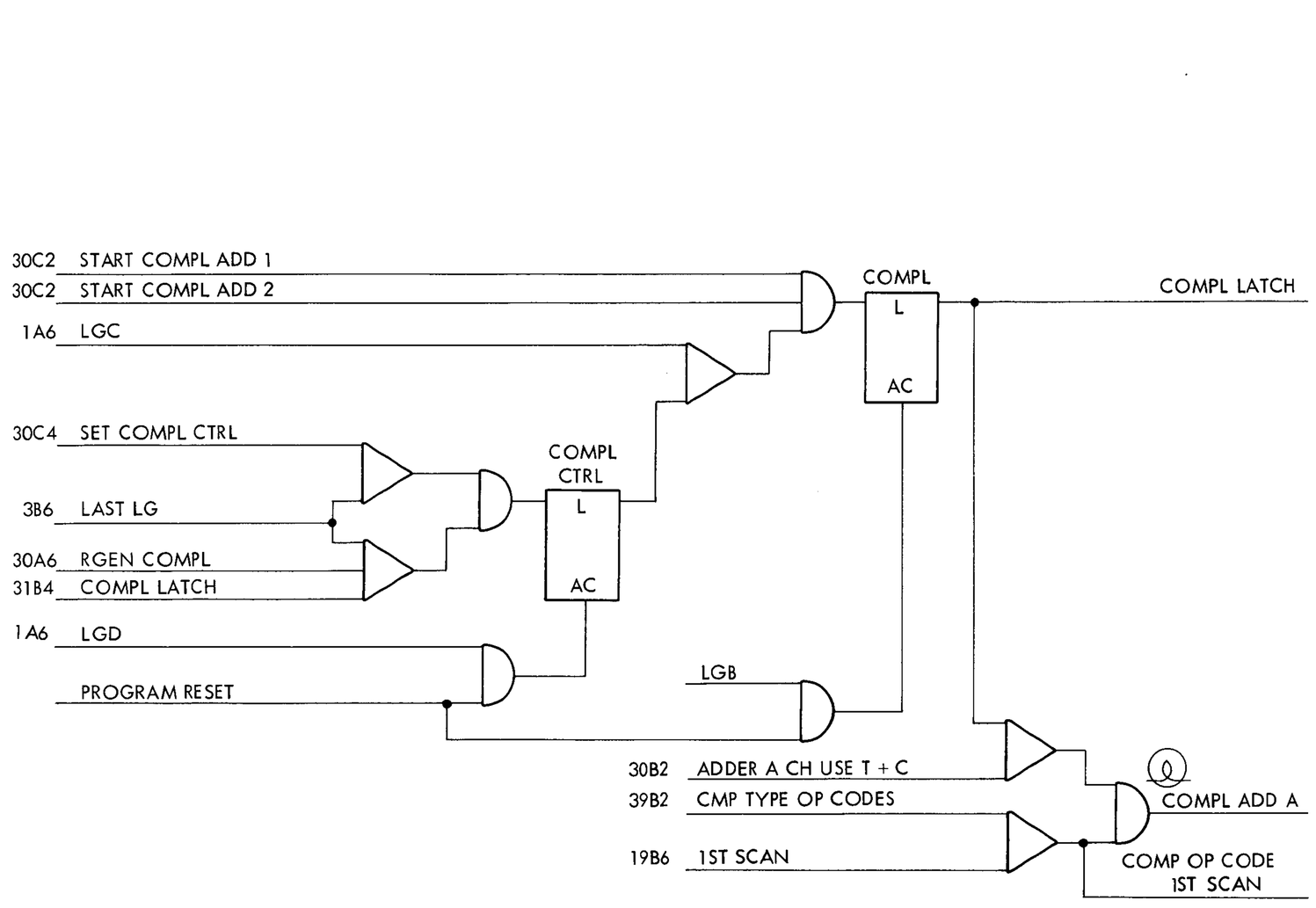
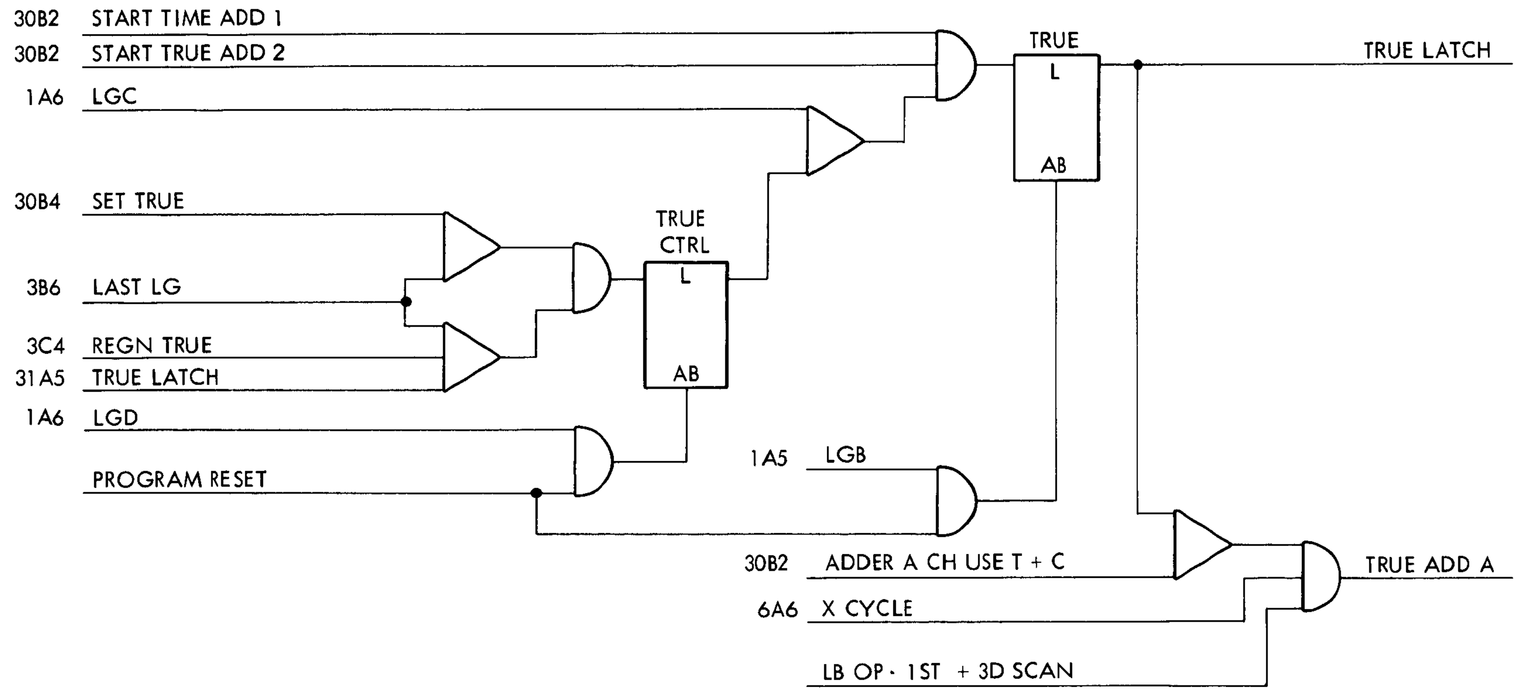
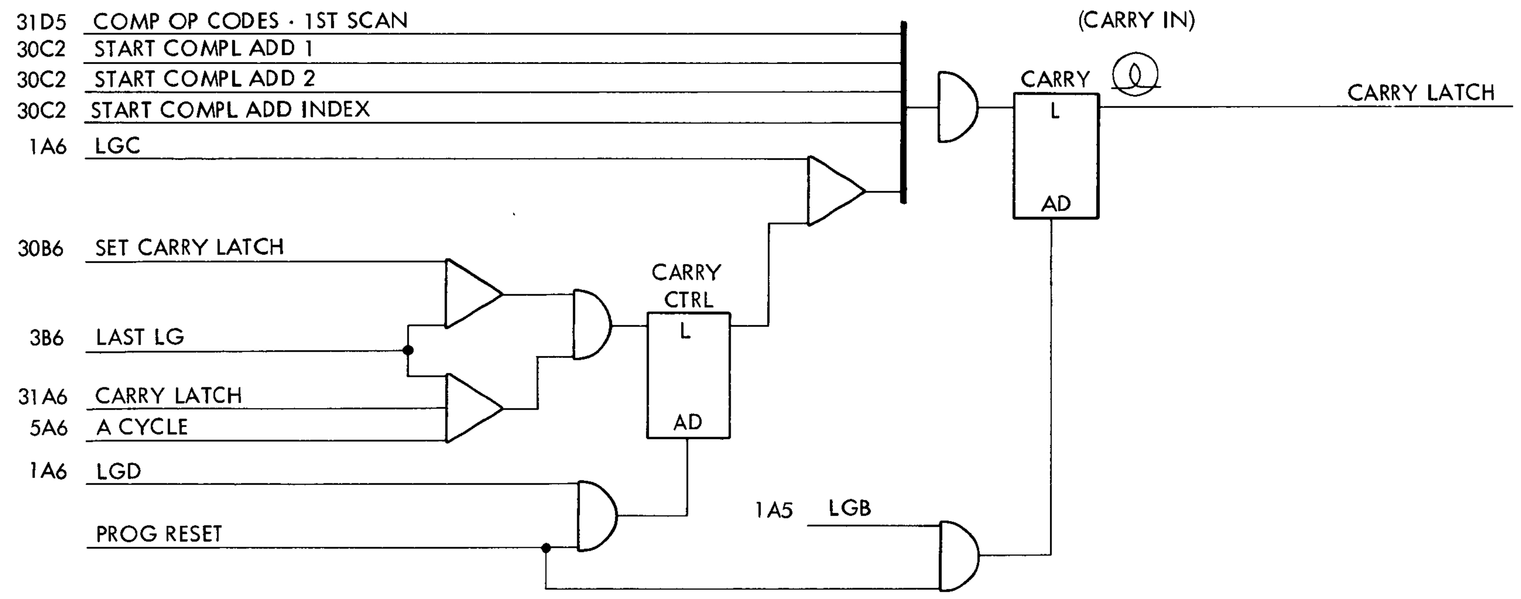
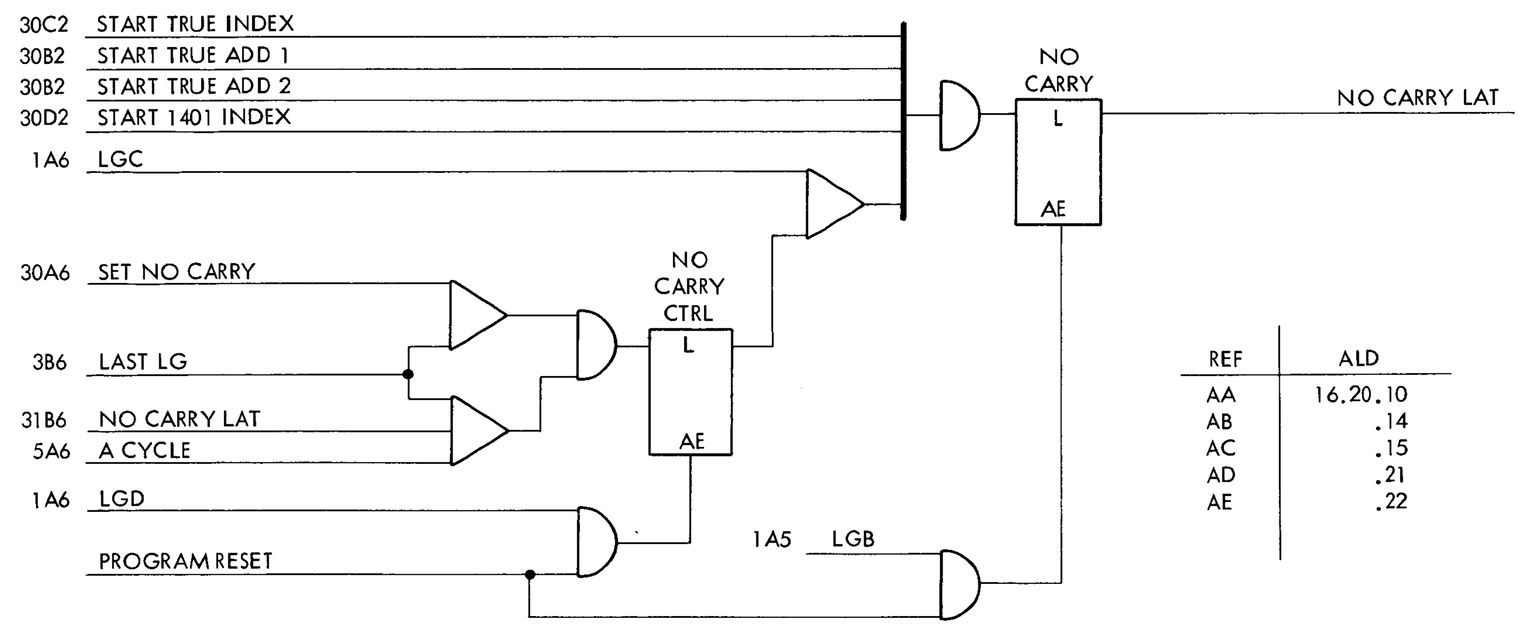


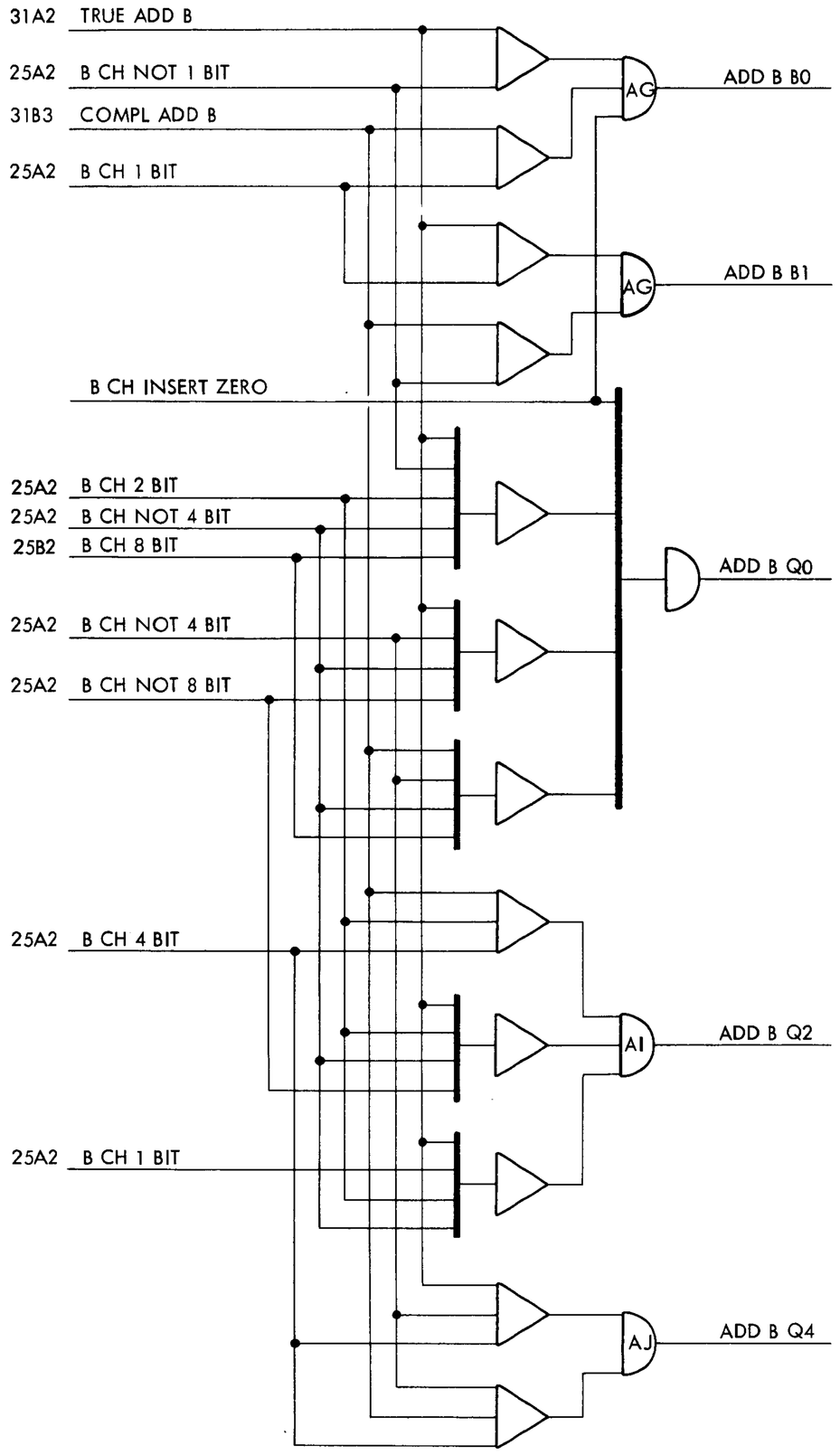
FIGURE 31. ADDER CTRL LATCHES

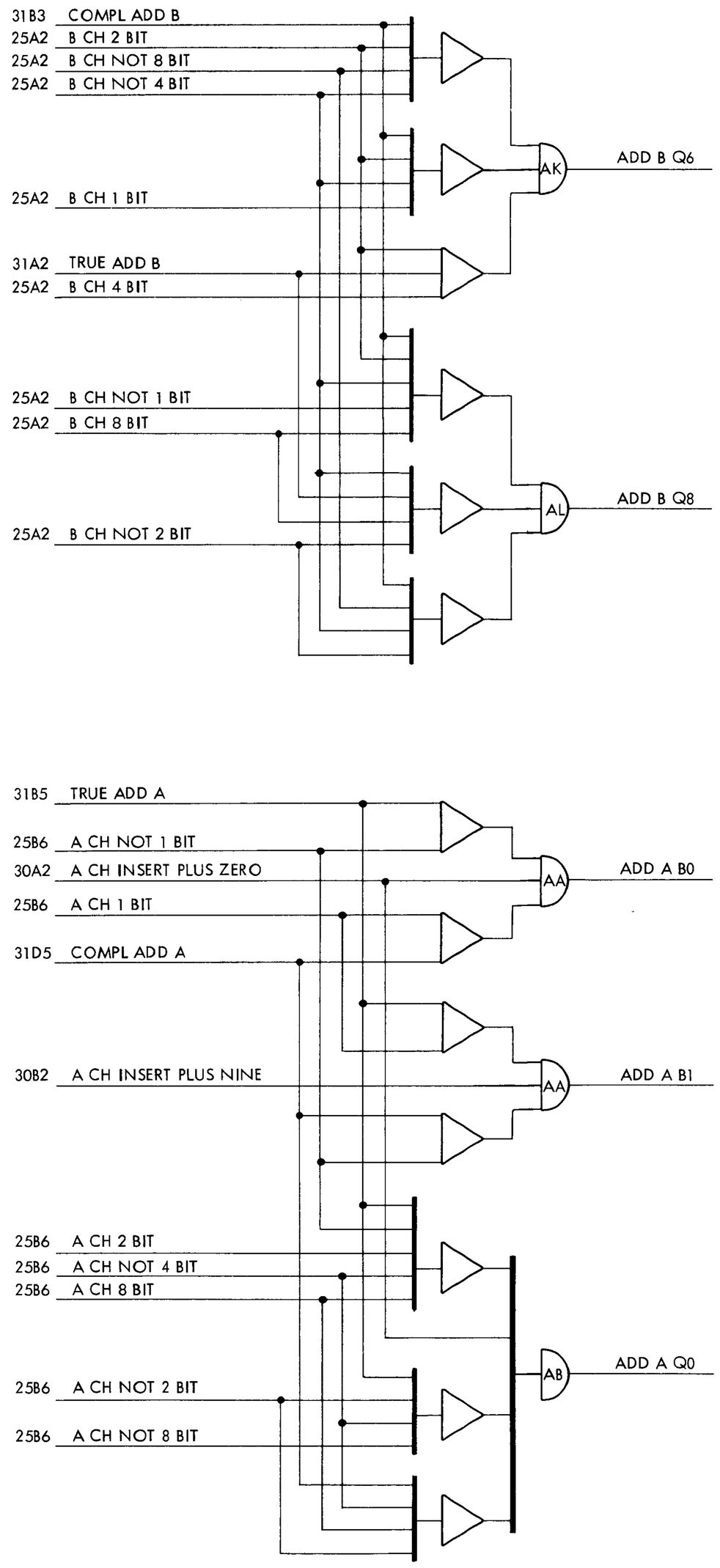


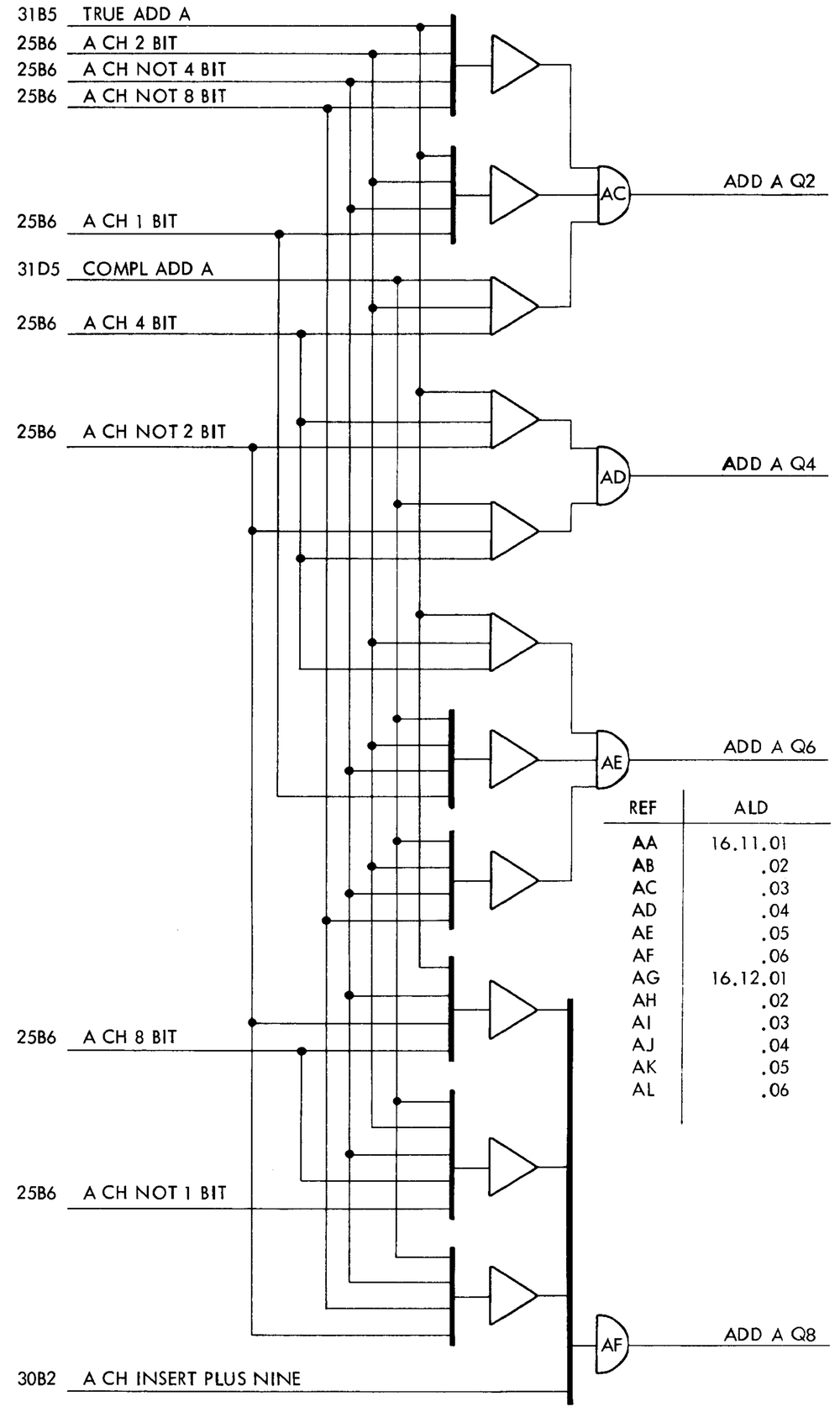




REF	ALD
AA	16.20.10
AB	.14
AC	.15
AD	.21
AE	.22

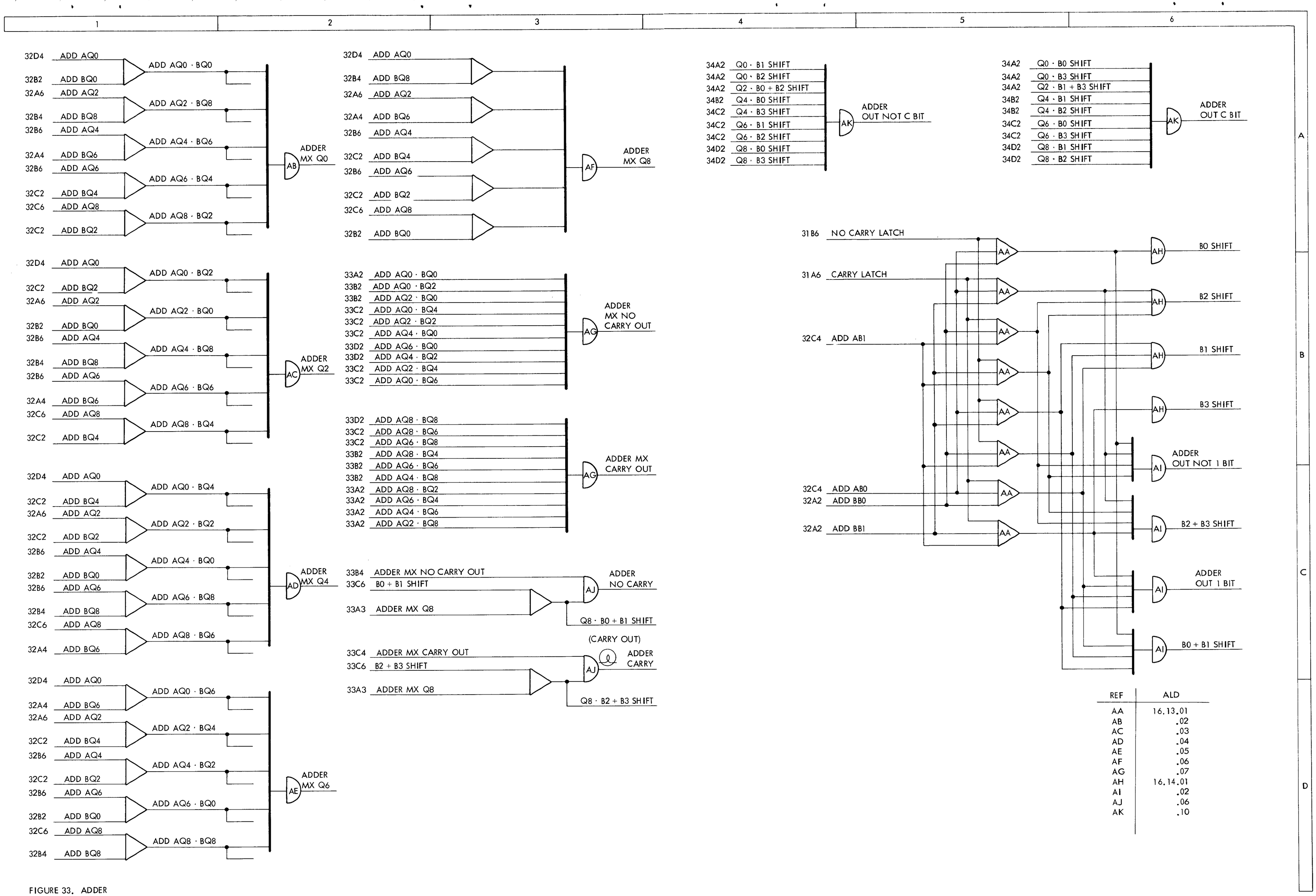






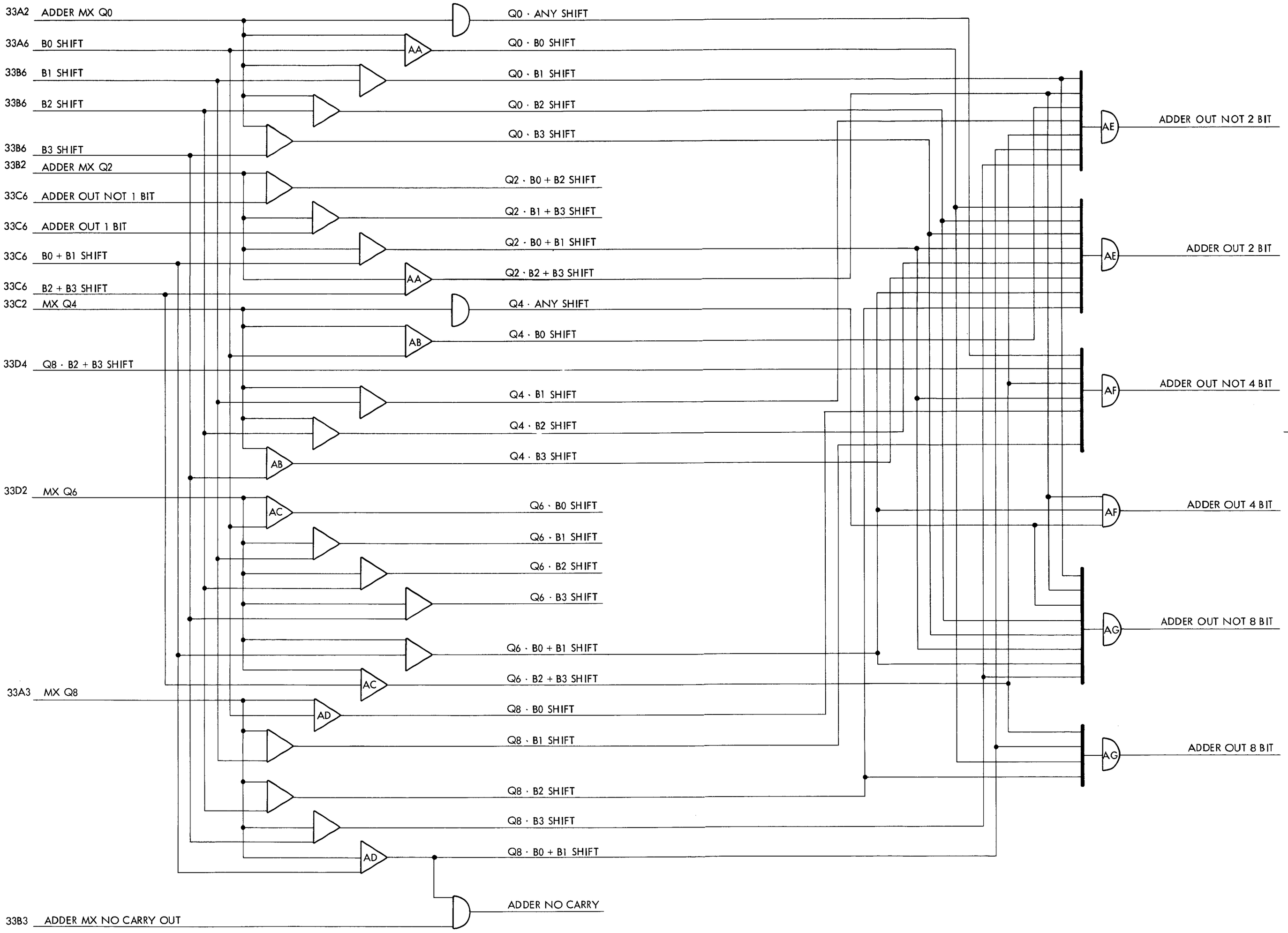
REF	ALD
AA	16.11.01
AB	.02
AC	.03
AD	.04
AE	.05
AF	.06
AG	16.12.01
AH	.02
AI	.03
AJ	.04
AK	.05
AL	.06

FIGURE 32. ADDER BCD TO QUI-BINARY



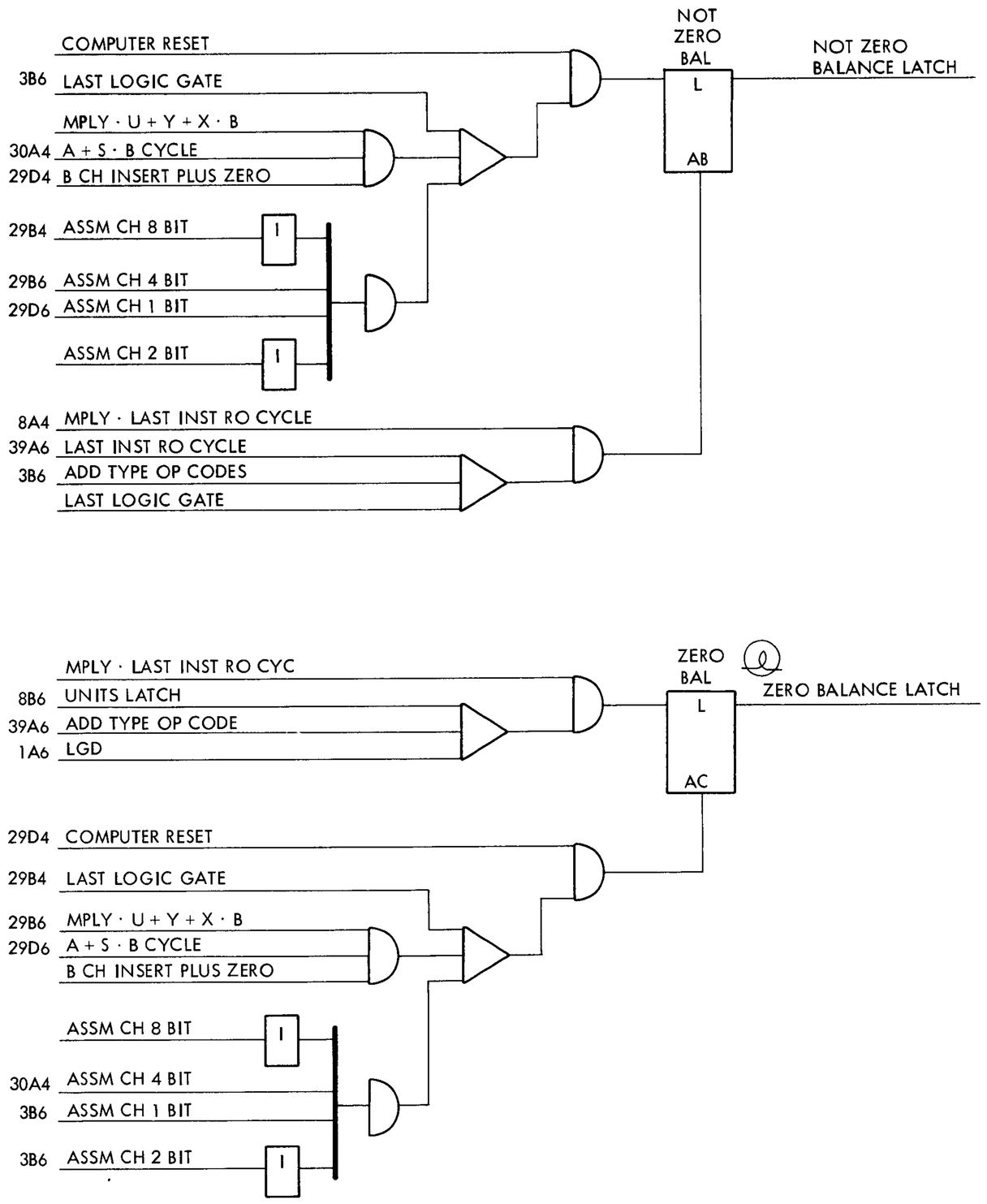
REF	ALD
AA	16.13.01
AB	.02
AC	.03
AD	.04
AE	.05
AF	.06
AG	.07
AH	16.14.01
AI	.02
AJ	.06
AK	.10

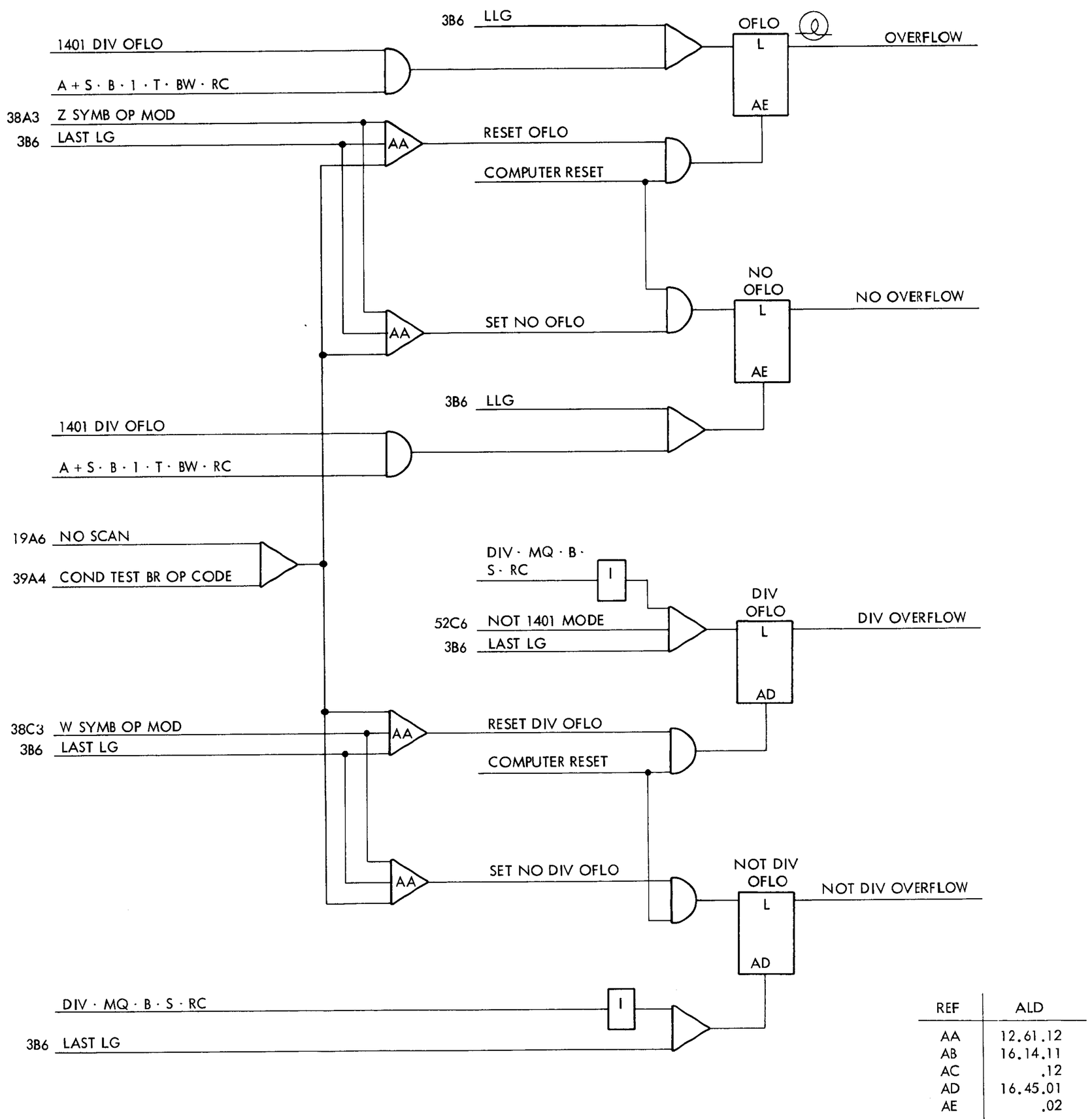
FIGURE 33. ADDER



REF	ALD
AA	16.14.03
AB	.04
AC	.05
AD	.06
AE	.07
AF	.08
AG	.09

FIGURE 34. ADDER OUT XLATOR





REF	ALD
AA	12.61.12
AB	16.14.11
AC	.12
AD	16.45.01
AE	.02

FIGURE 35. ZERO BAL, OFLO, AND DIV OFLO LATCHES

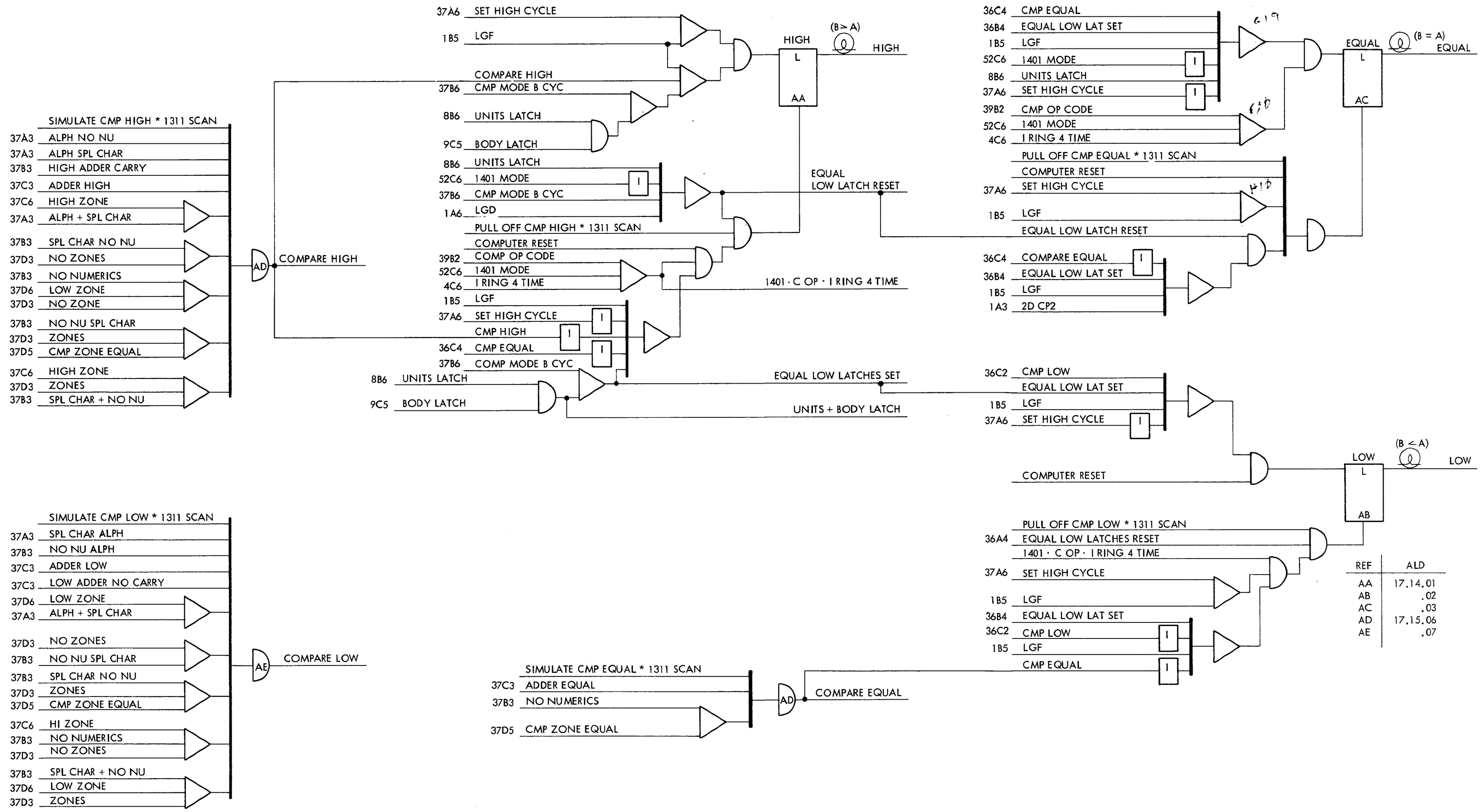


FIGURE 36. HIGH, LOW, EQUAL COMPARE LATCHES

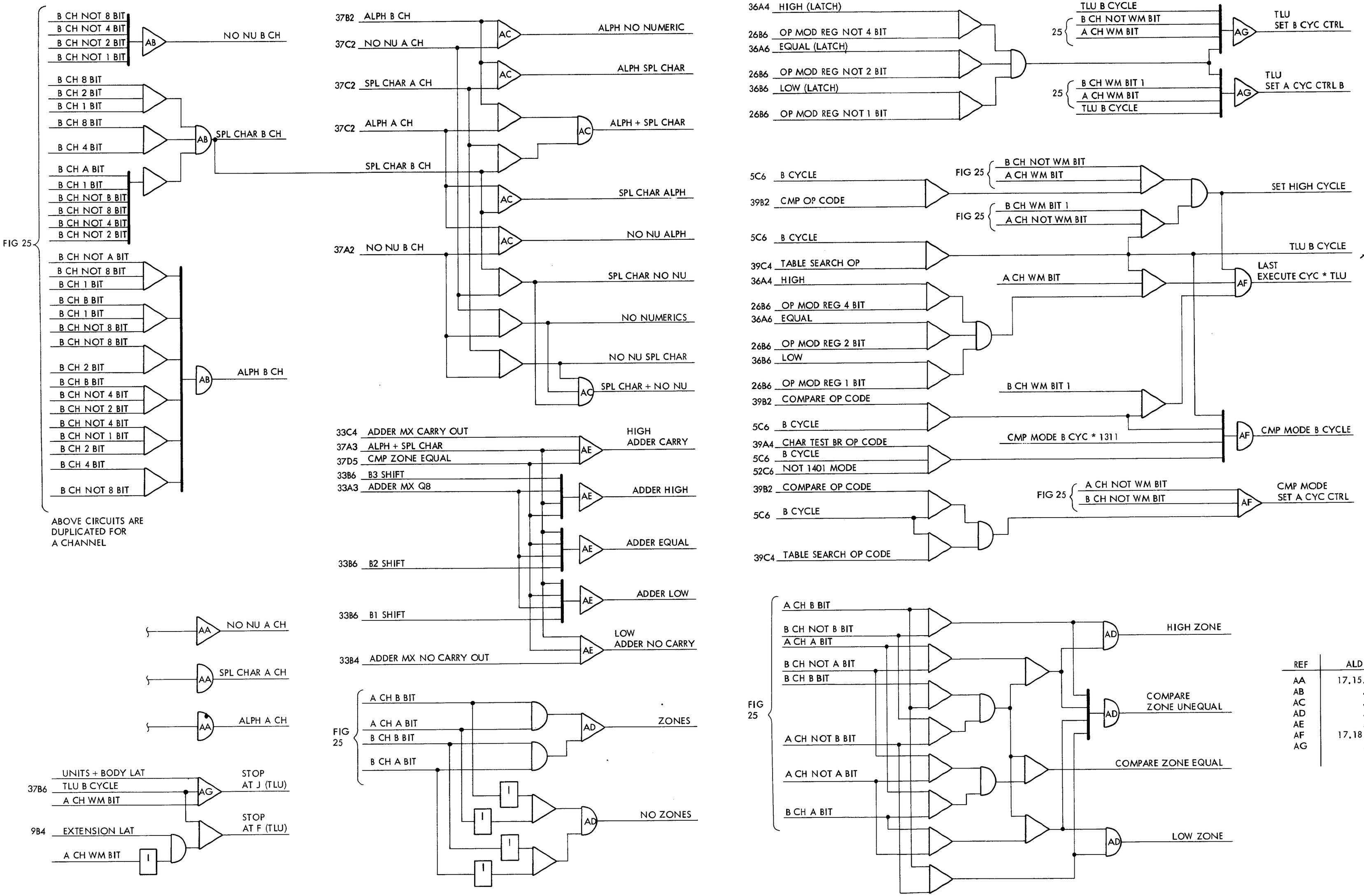
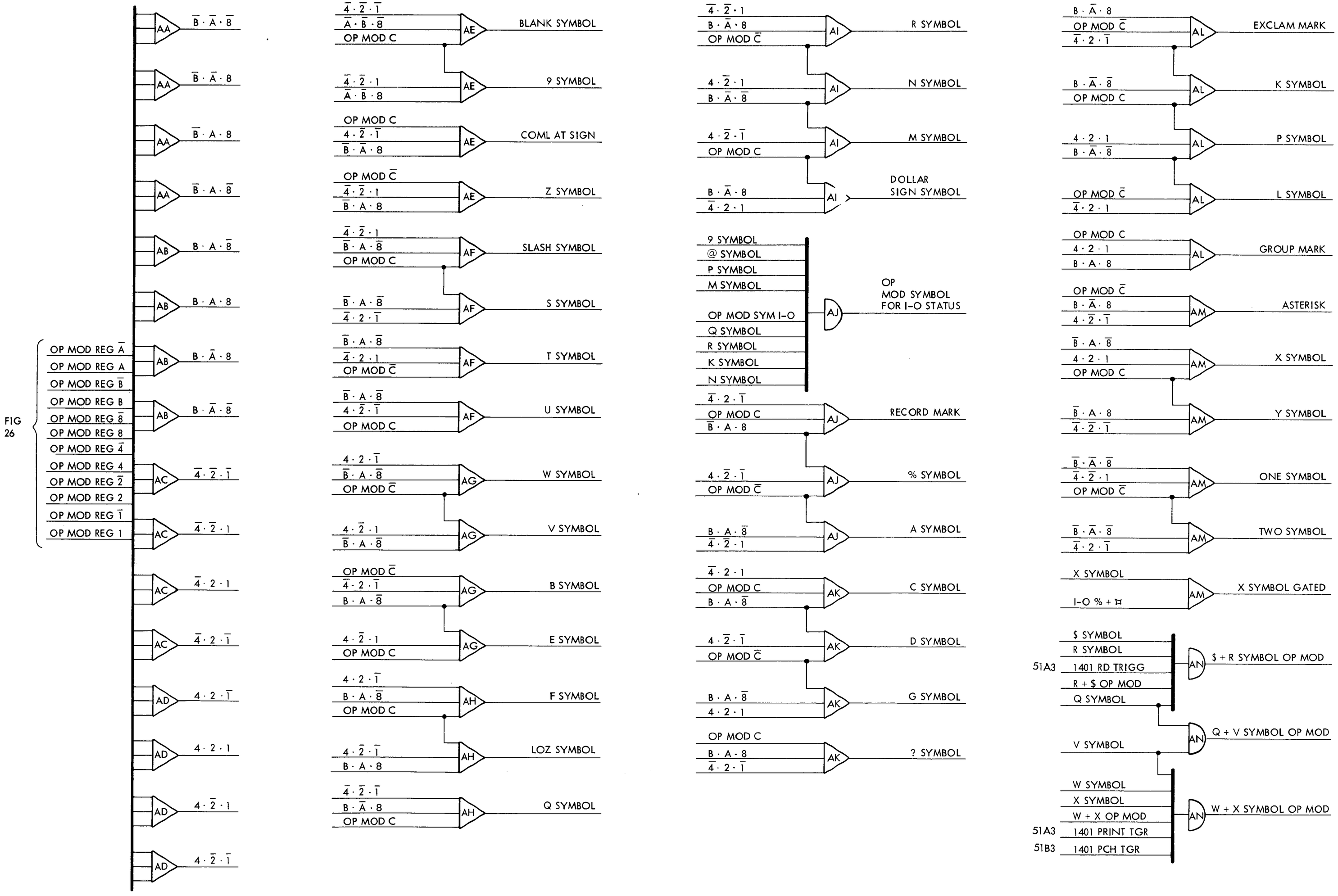
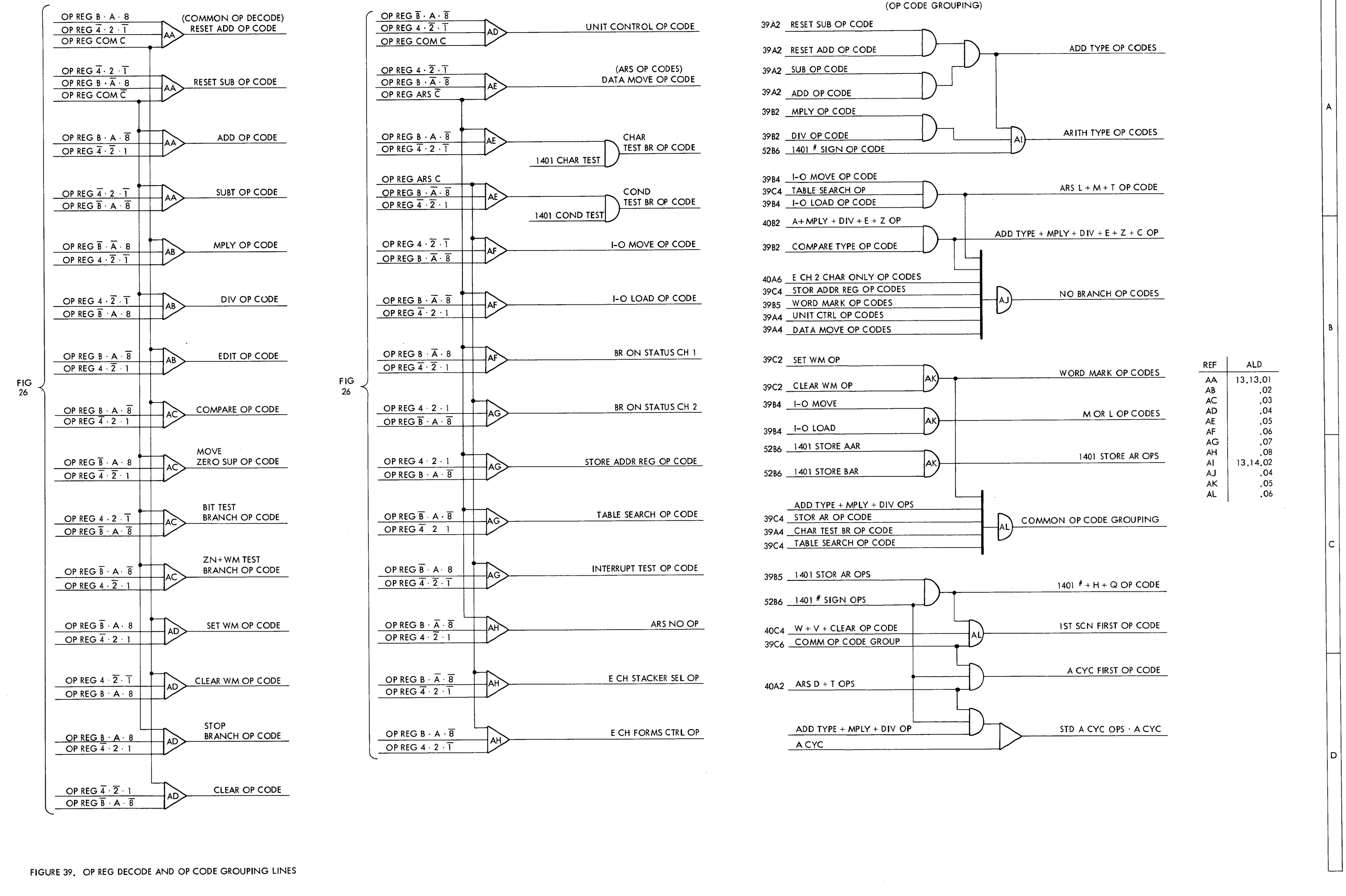


FIGURE 37. COMPARE AND TLU



REF	ALD
AA	13,12,05
AB	.06
AC	.07
AD	.08
AE	.09
AF	.10
AG	13,12,11
AH	.12
AI	.13
AJ	.14
AK	.15
AL	.16
AM	.17
AN	.18

FIGURE 38. OP MOD DECODE



REF	ALD
AA	13,13.01
AB	.02
AC	.03
AD	.04
AE	.05
AF	.06
AG	.07
AH	.08
AI	13,14.02
AJ	.04
AK	.05
AL	.06

FIGURE 39. OP REG DECODE AND OP CODE GROUPING LINES

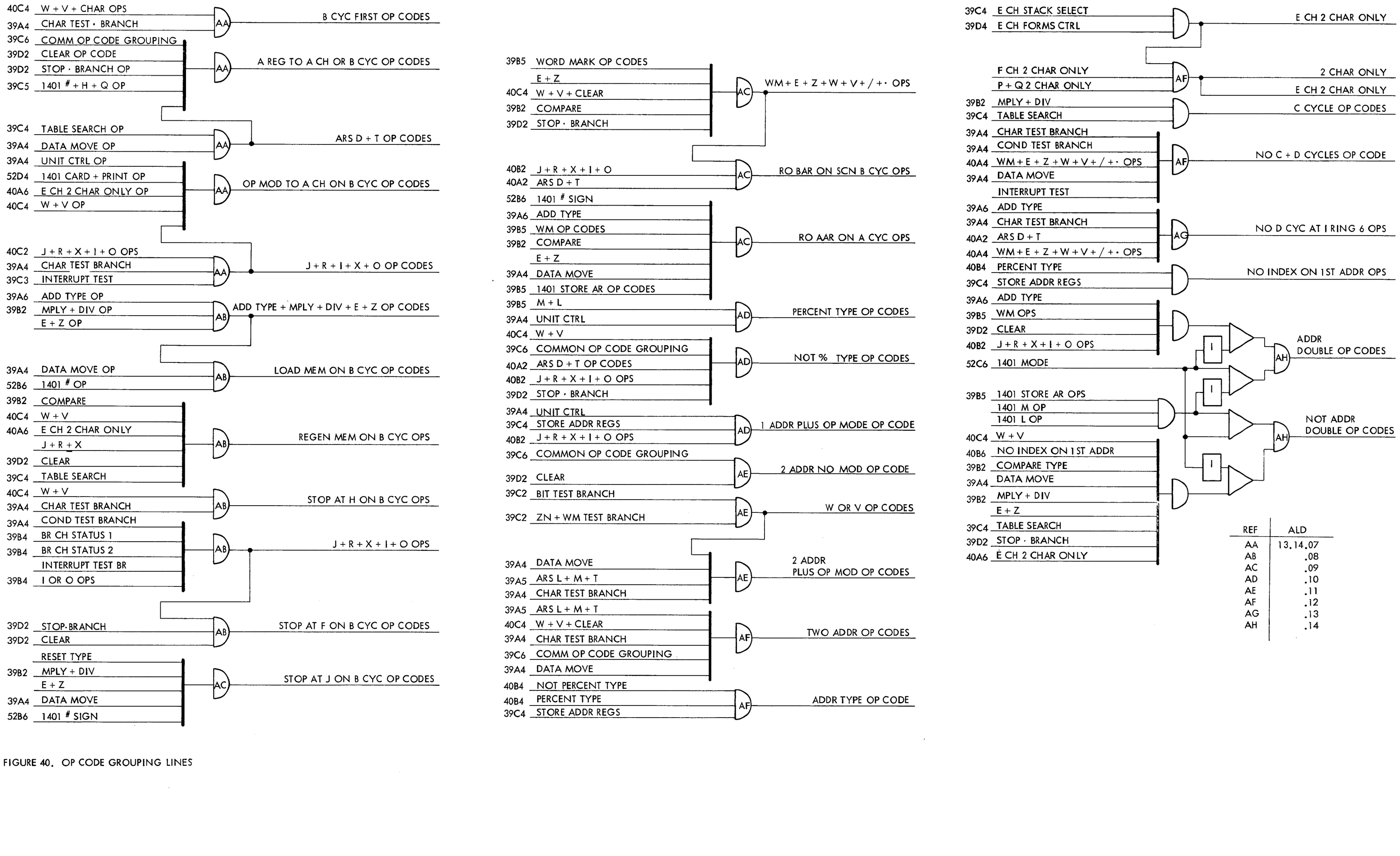
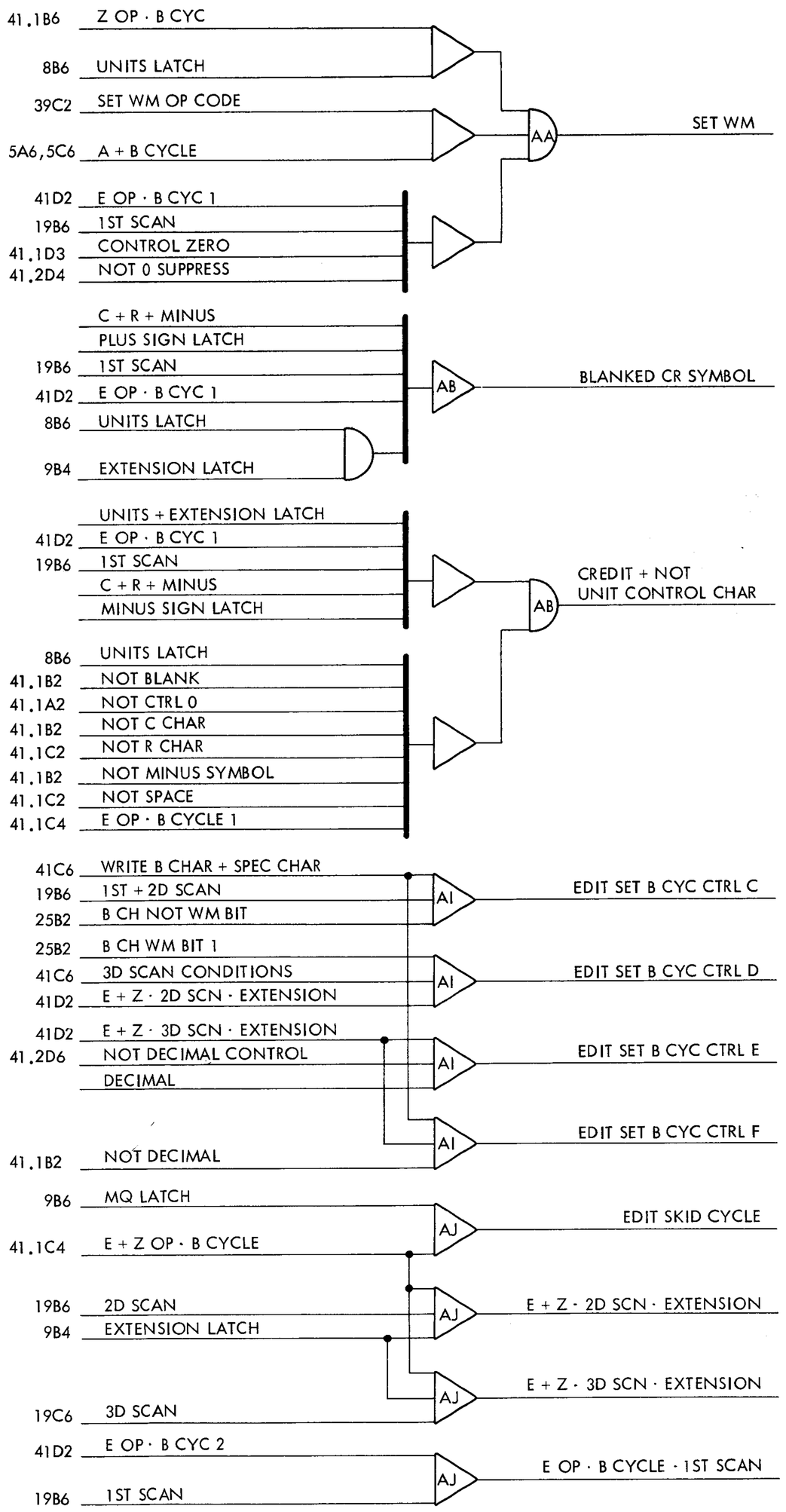
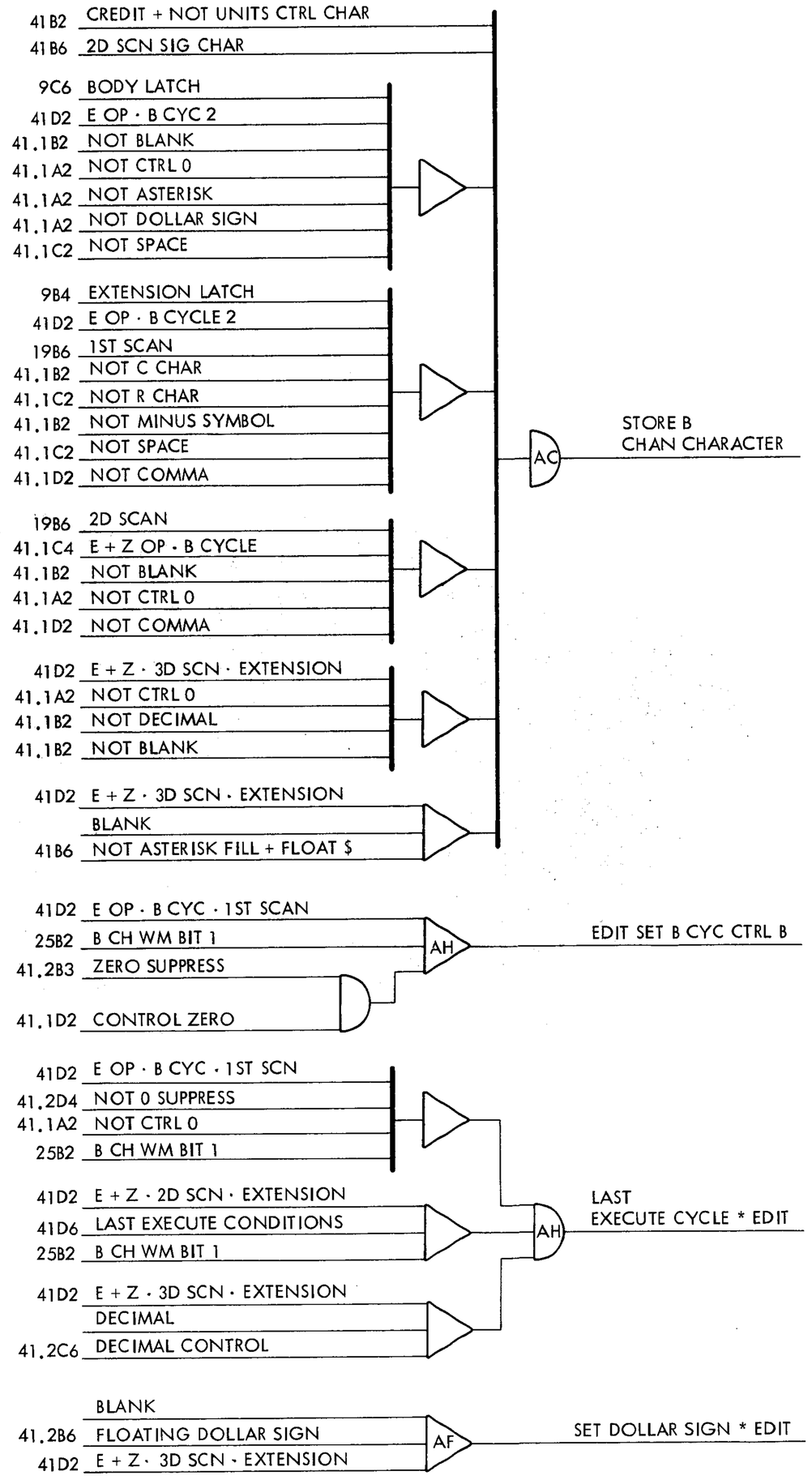
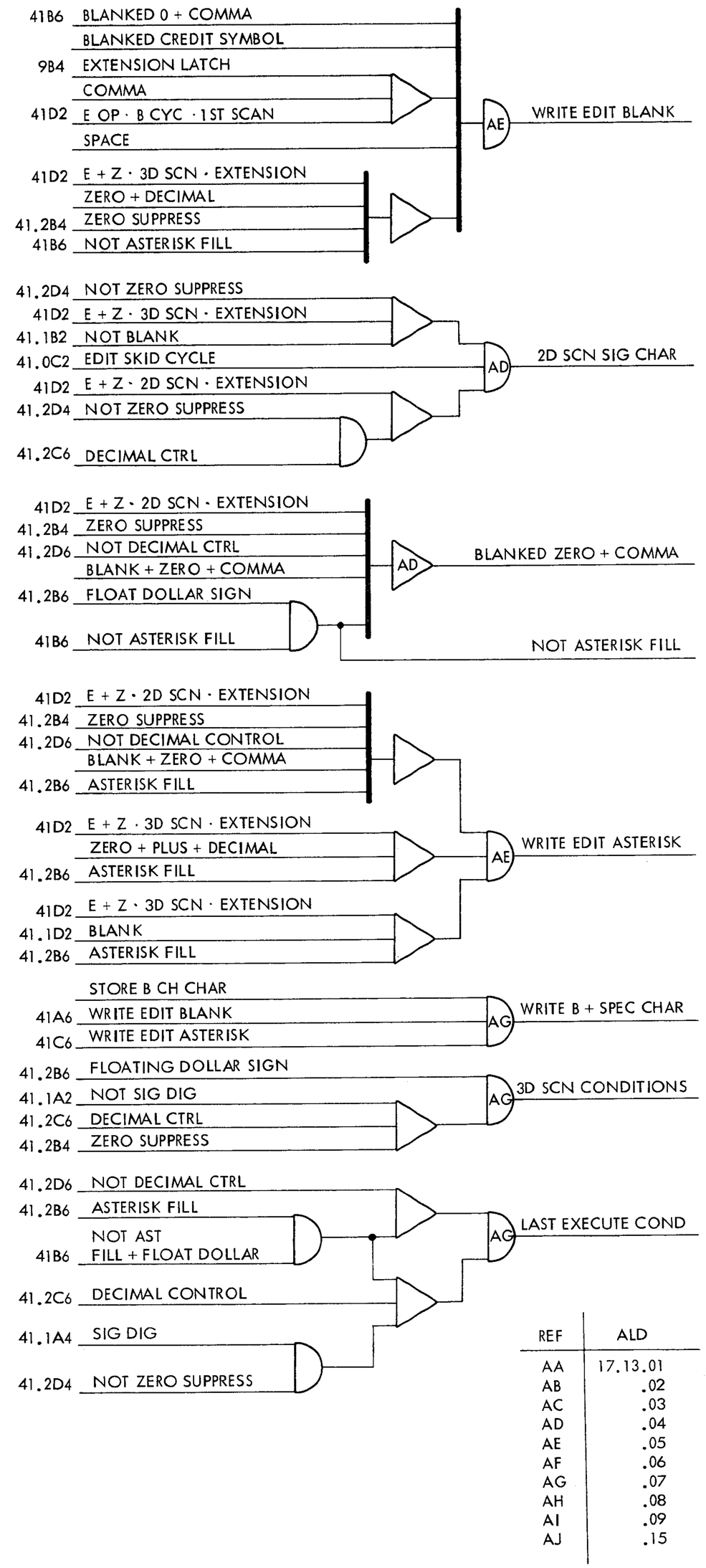


FIGURE 40. OP CODE GROUPING LINES

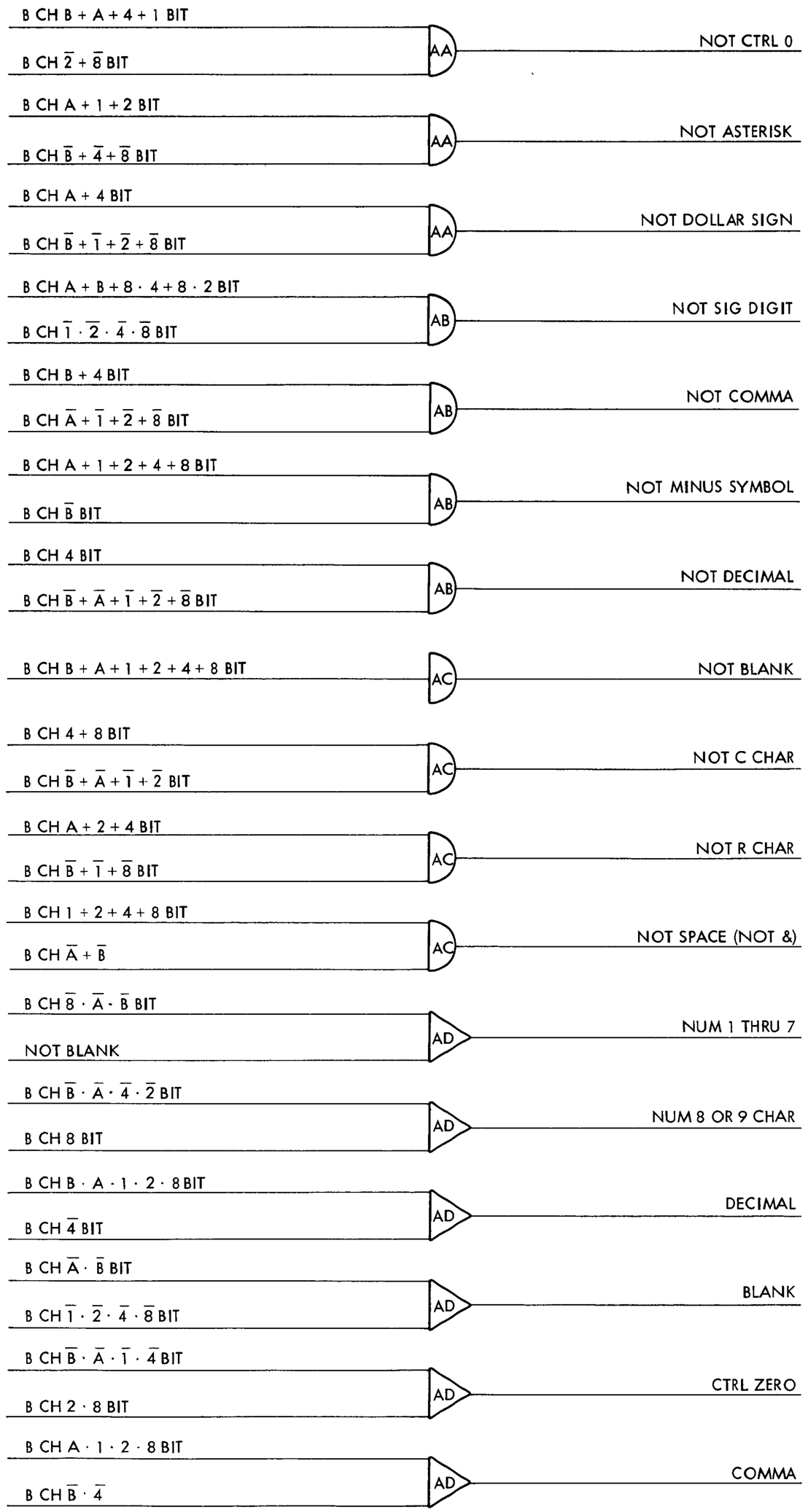


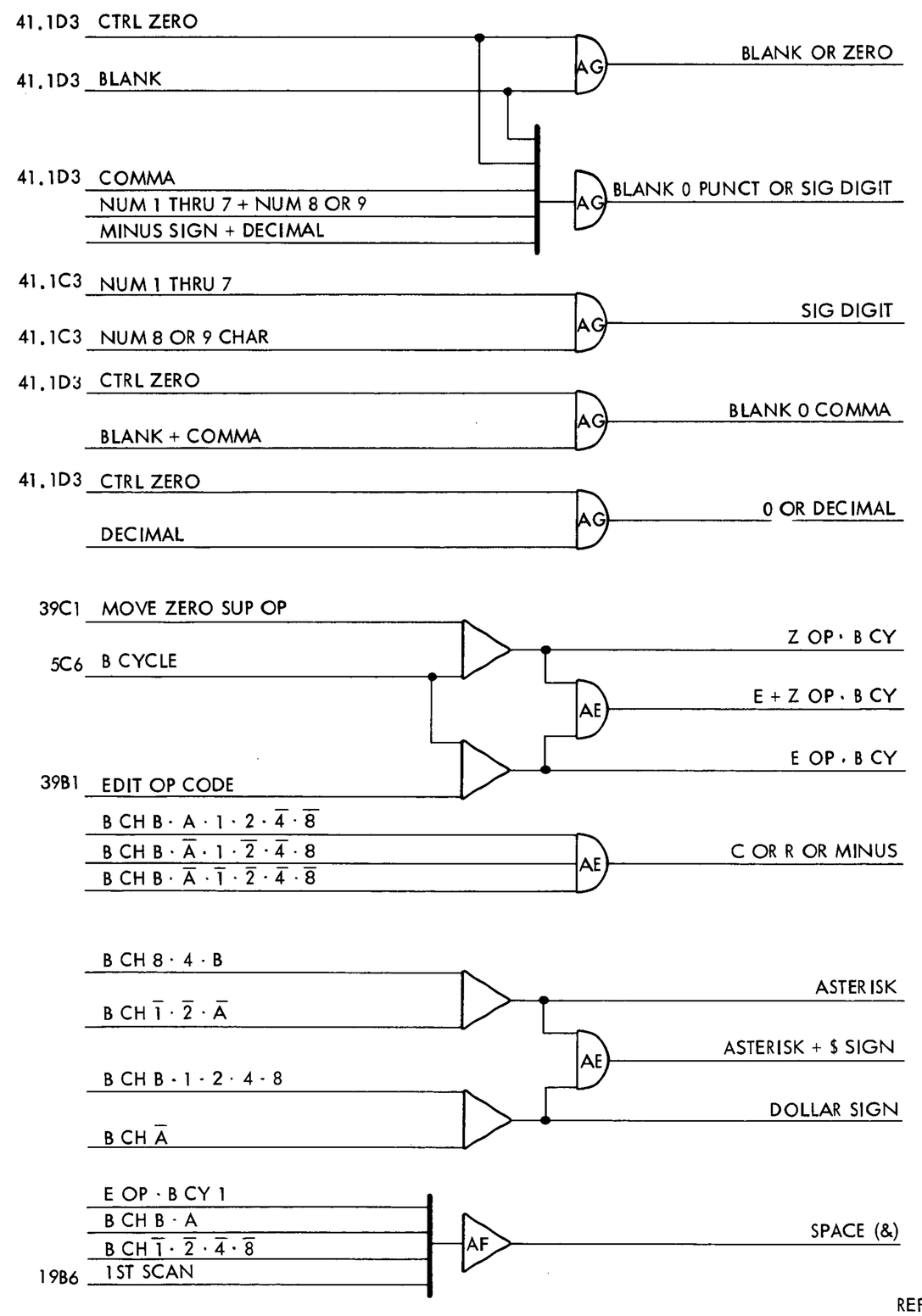




REF	ALD
AA	17.13.01
AB	.02
AC	.03
AD	.04
AE	.05
AF	.06
AG	.07
AH	.08
AI	.09
AJ	.15

FIGURE 41.0 EDIT CONTROL





REF	ALD
AA	17.11.01
AB	17.11.02
AC	17.11.03
AD	17.11.05
AE	17.11.04
AF	17.11.07
AG	17.11.06

FIGURE 41.1 EDIT TRANSL

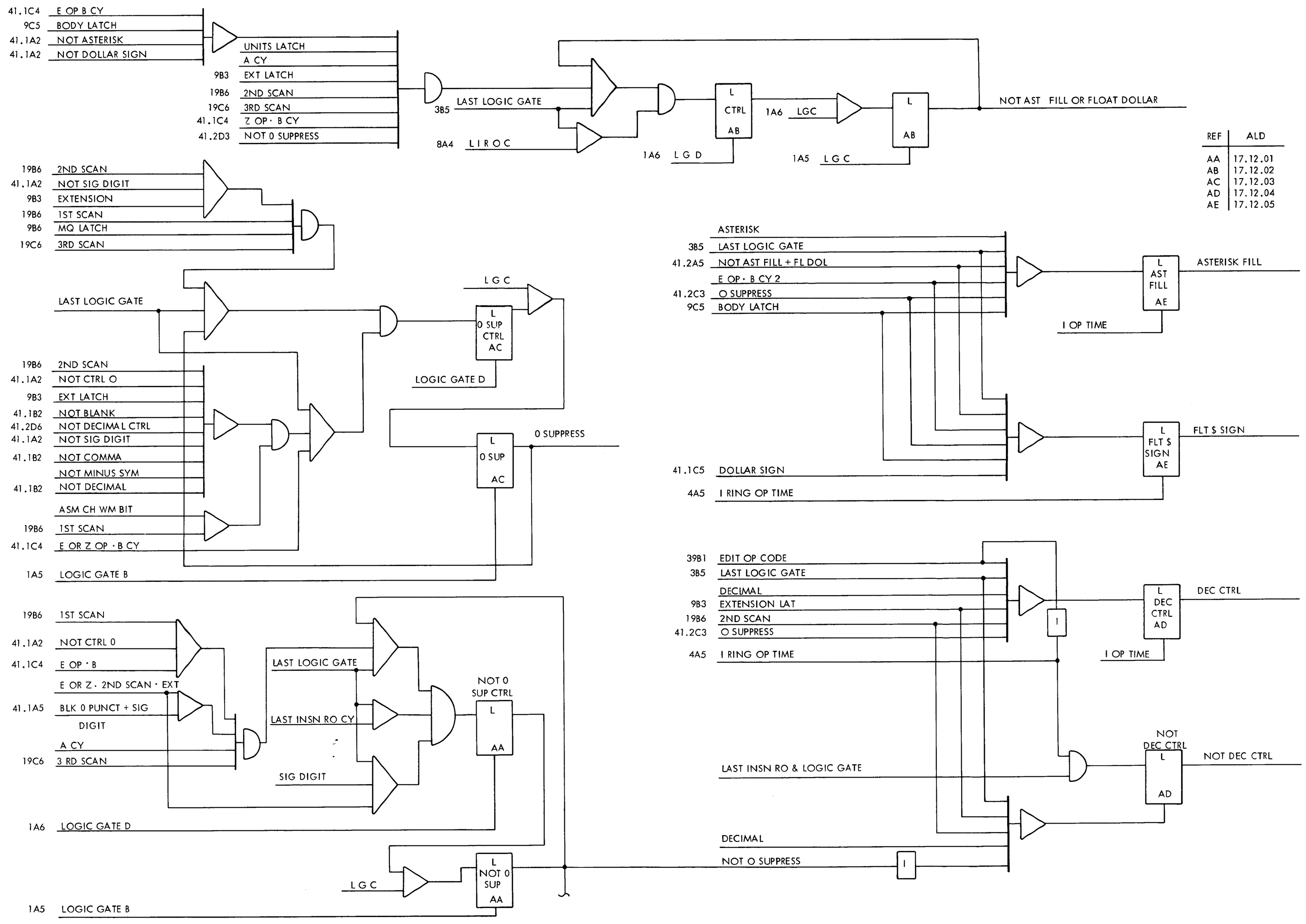
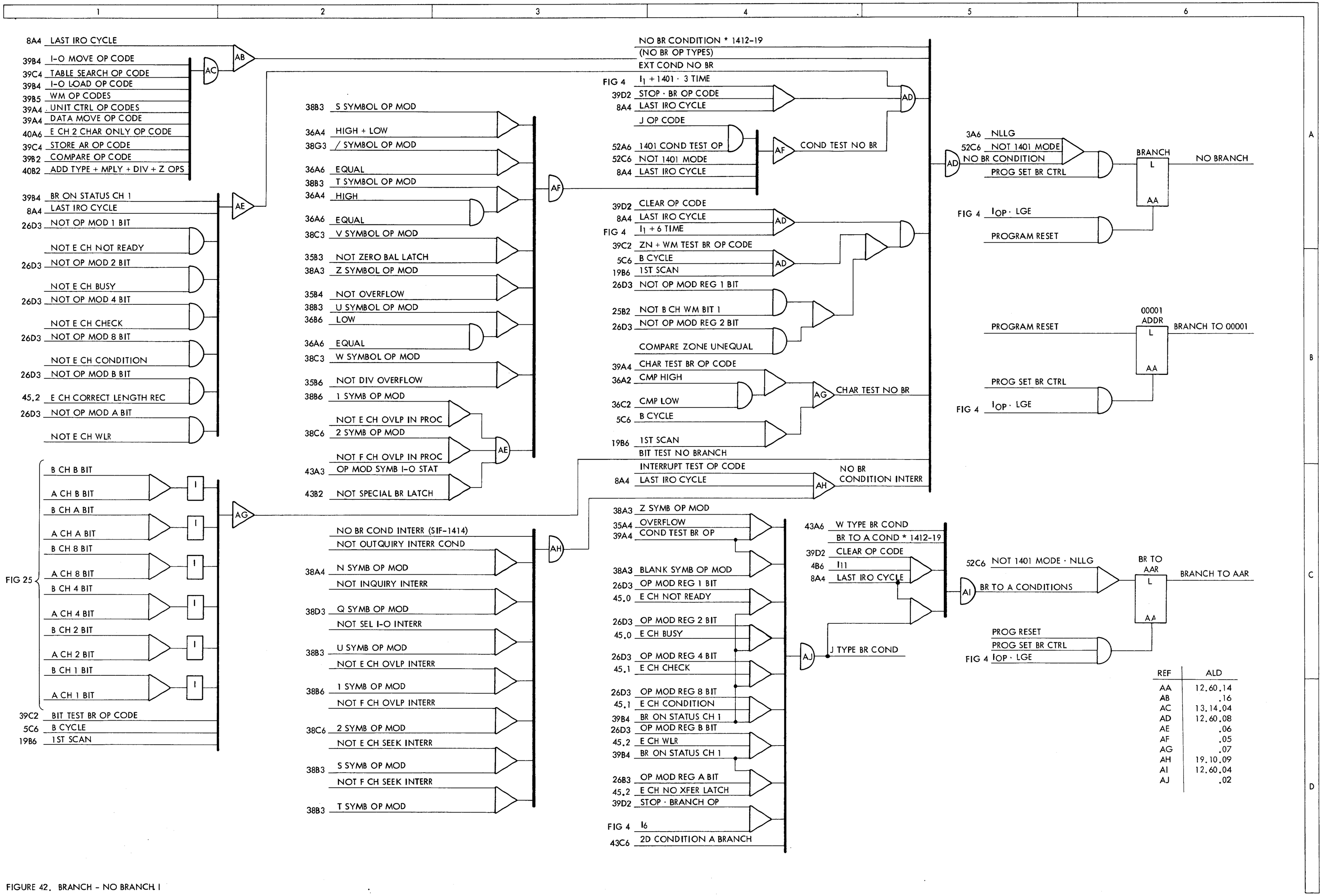


FIGURE 41.2. EDIT LATCHES



REF	ALD
AA	12.60.14
AB	.16
AC	13.14.04
AD	12.60.08
AE	.06
AF	.05
AG	.07
AH	19.10.09
AI	12.60.04
AJ	.02

FIGURE 42. BRANCH - NO BRANCH I

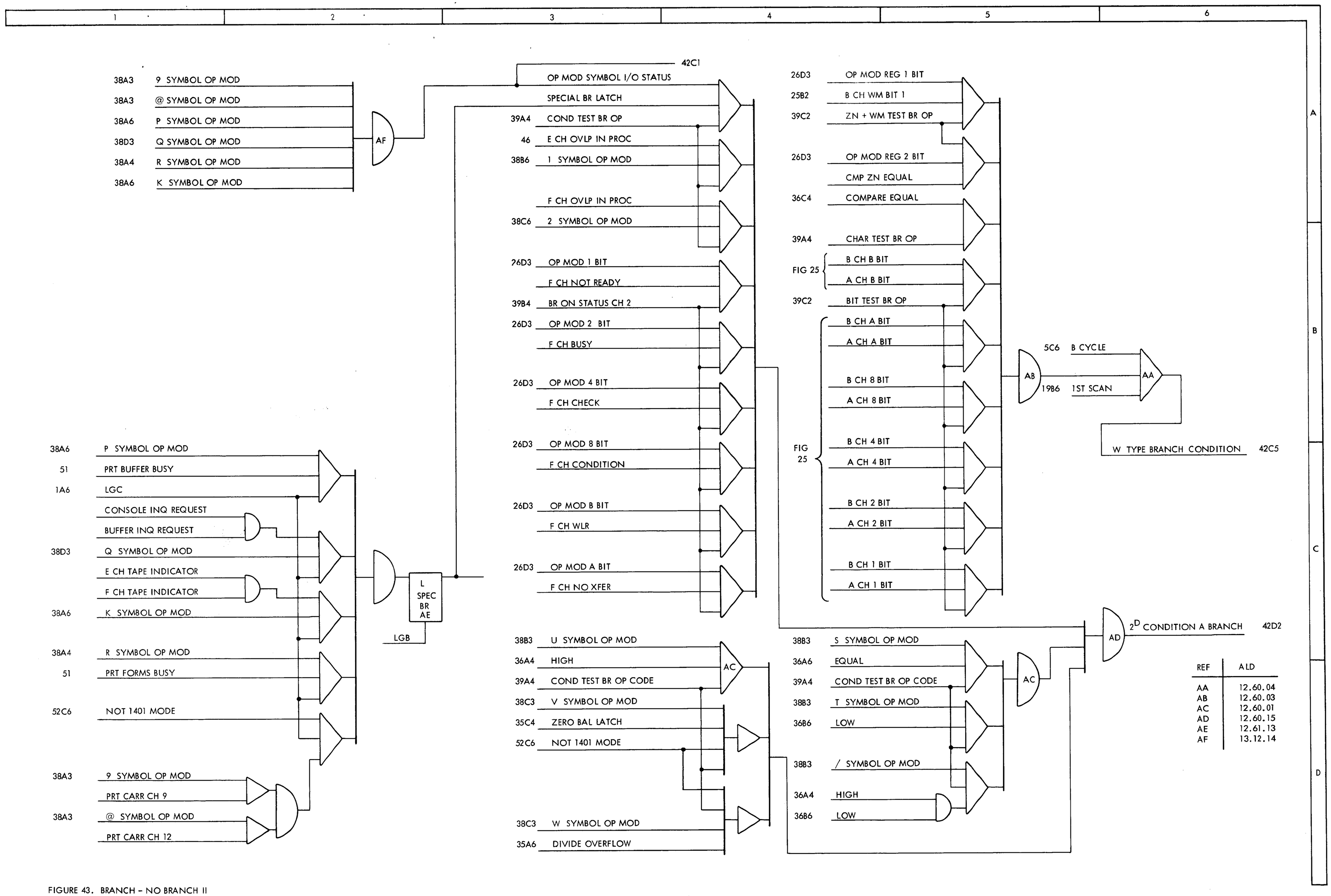


FIGURE 43. BRANCH - NO BRANCH II

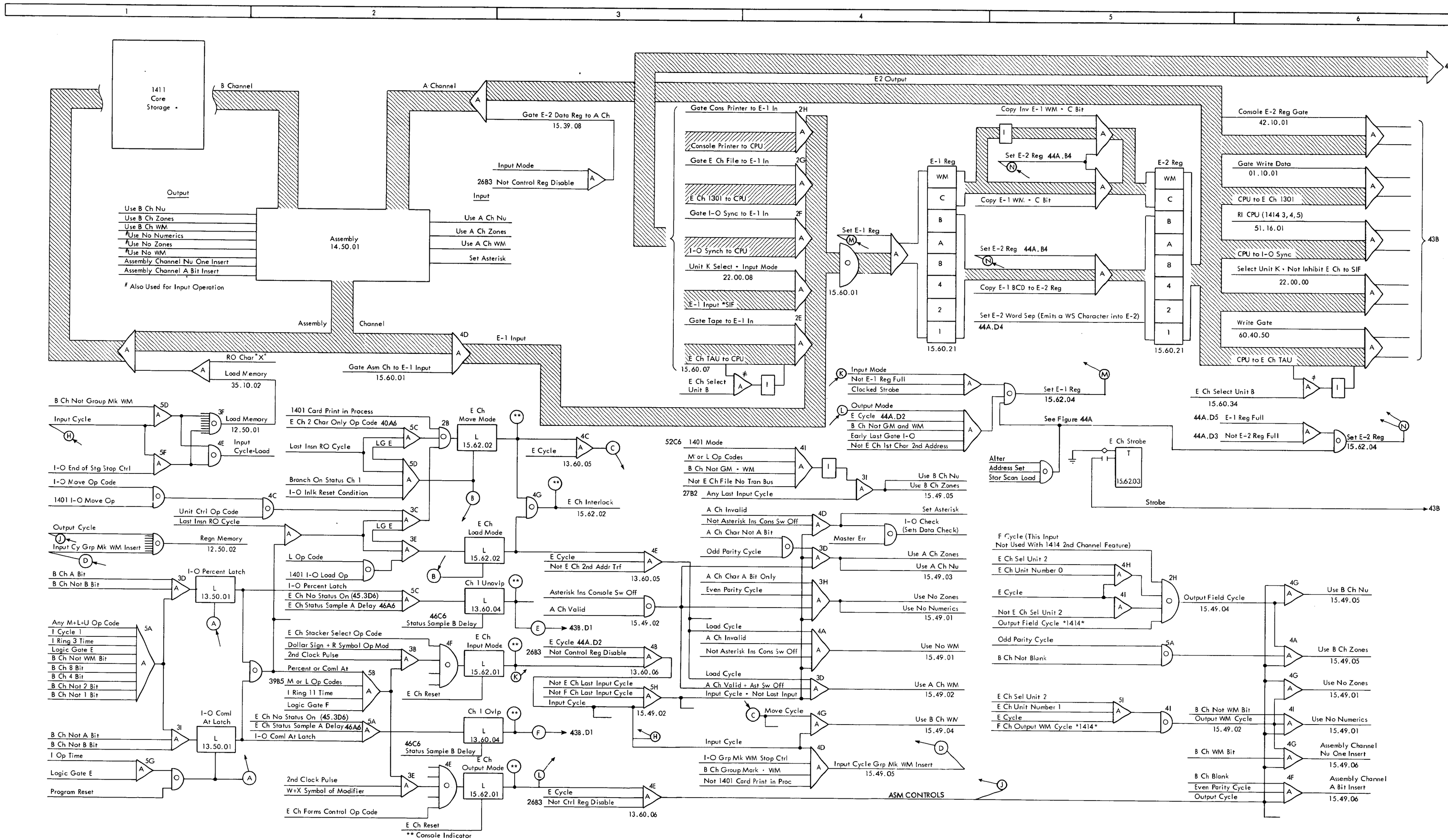


FIGURE 43.A. I-O DATA FLOW

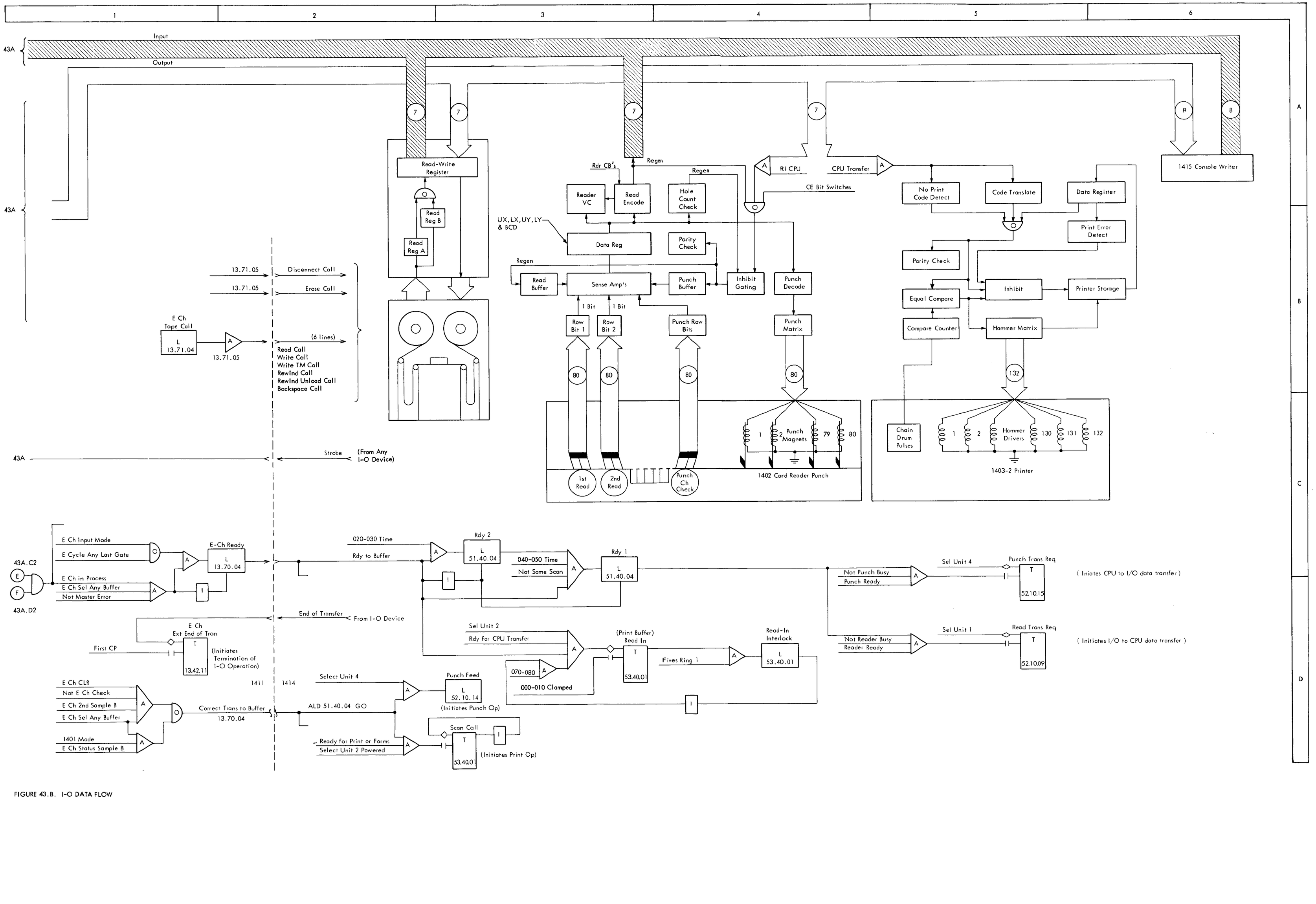


FIGURE 43.B. I-O DATA FLOW

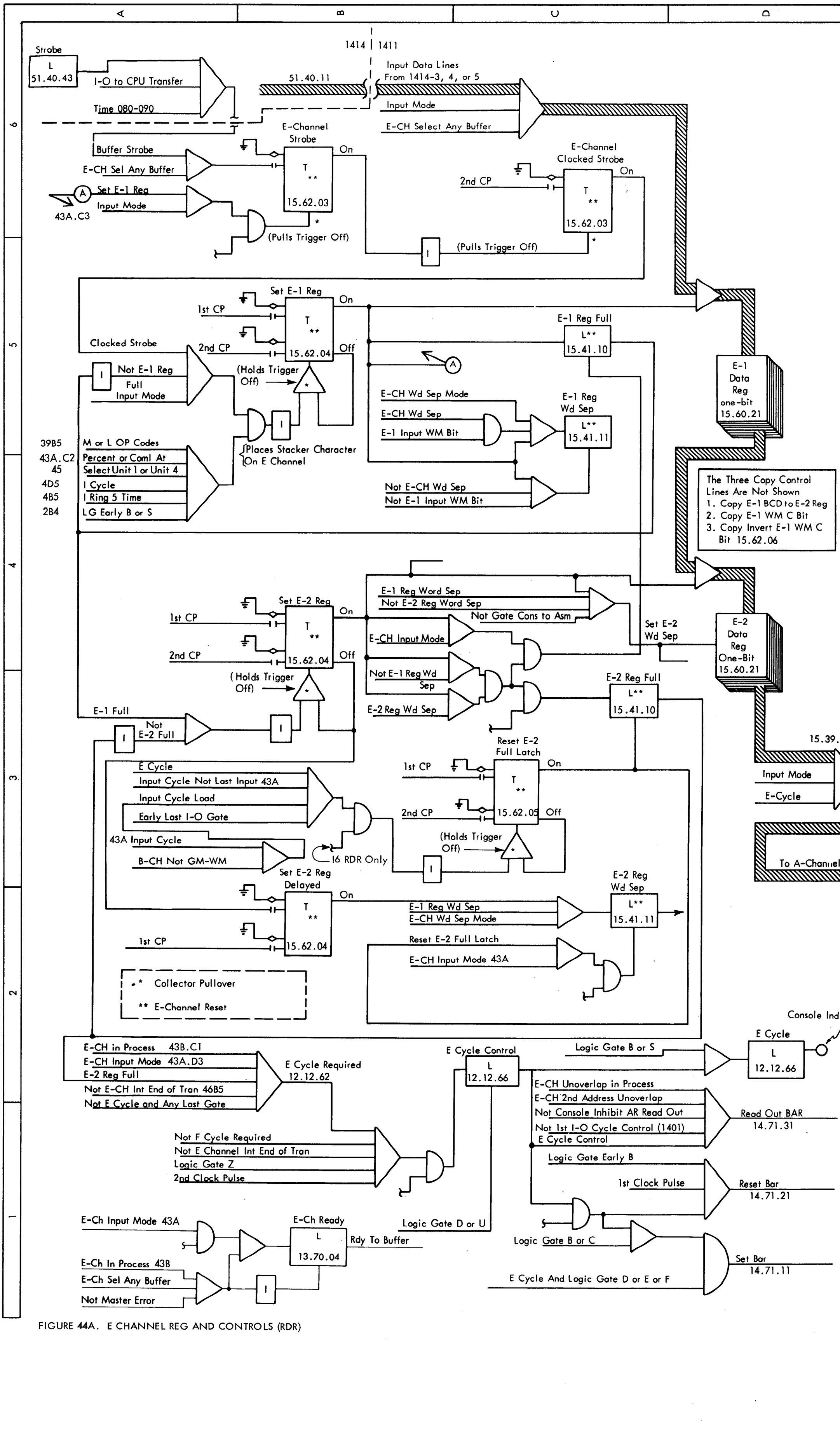
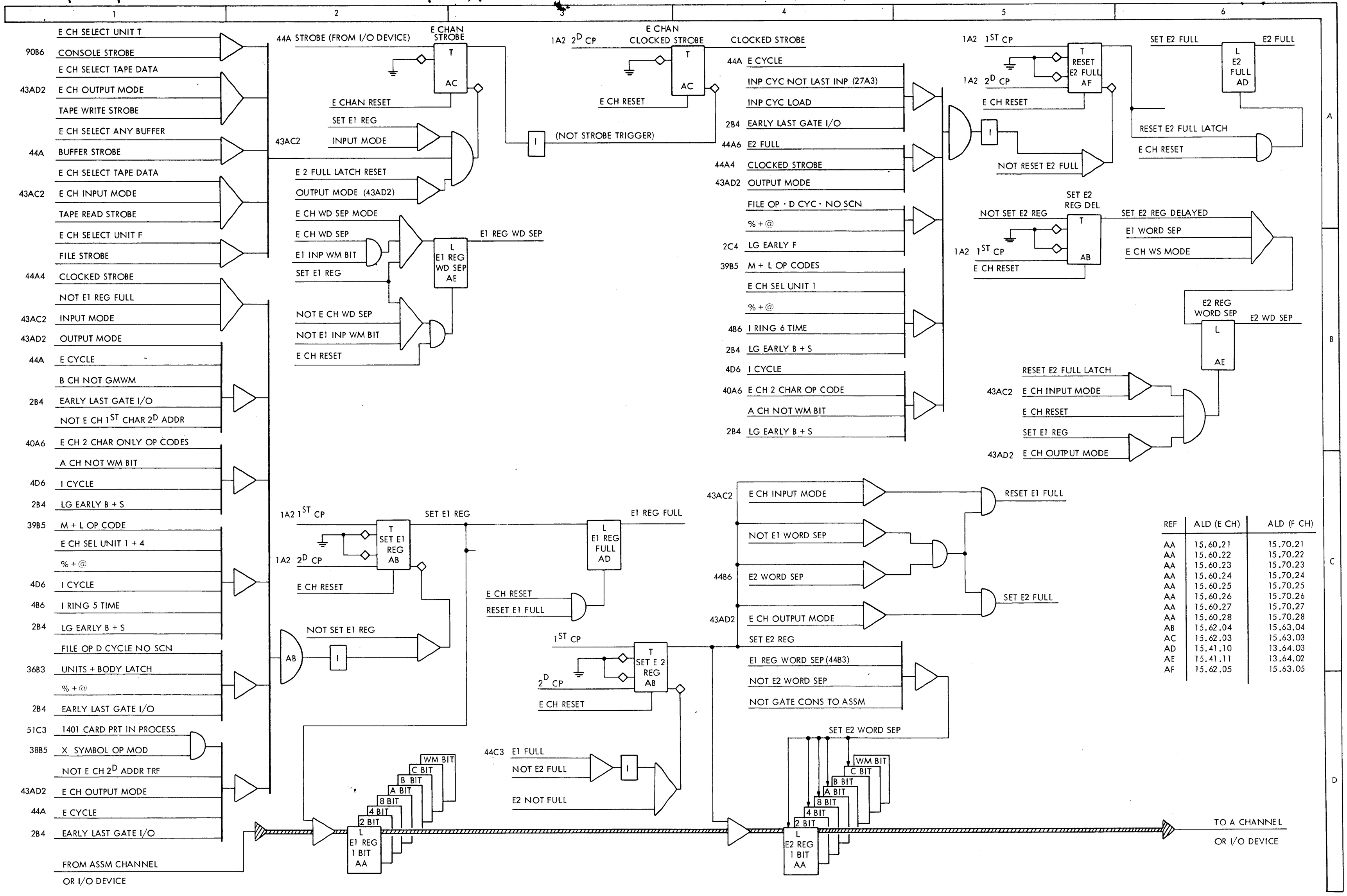


FIGURE 44A. E CHANNEL REG AND CONTROLS (RDR)



REF	ALD (E CH)	ALD (F CH)
AA	15.60.21	15.70.21
AA	15.60.22	15.70.22
AA	15.60.23	15.70.23
AA	15.60.24	15.70.24
AA	15.60.25	15.70.25
AA	15.60.26	15.70.26
AA	15.60.27	15.70.27
AA	15.60.28	15.70.28
AB	15.62.04	15.63.04
AC	15.62.03	15.63.03
AD	15.41.10	13.64.03
AE	15.41.11	13.64.02
AF	15.62.05	15.63.05

FIGURE 44. E & F CHAN REG & CTRL

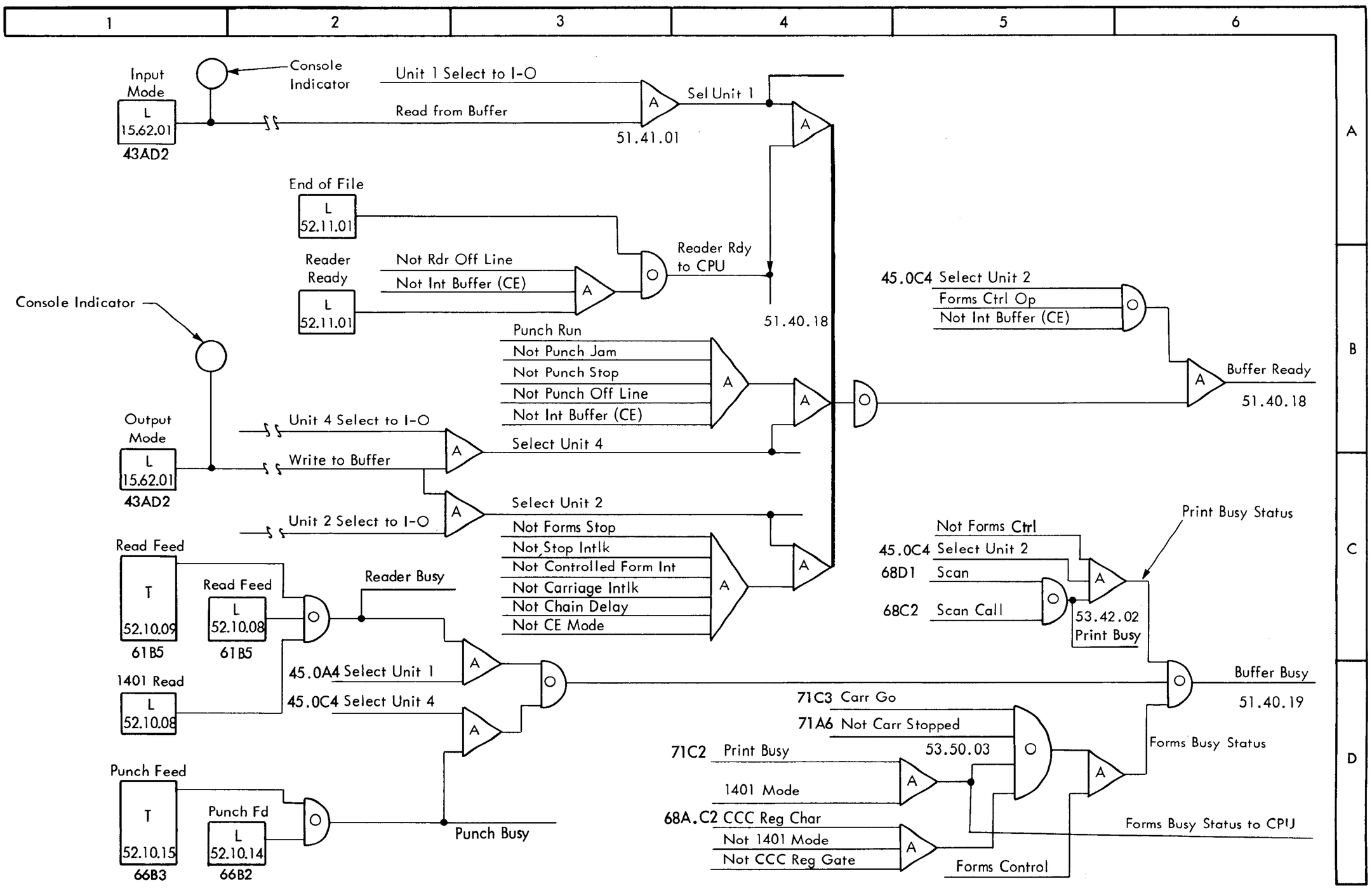


FIGURE 45.0. CHANNEL NOT READY OR BUSY

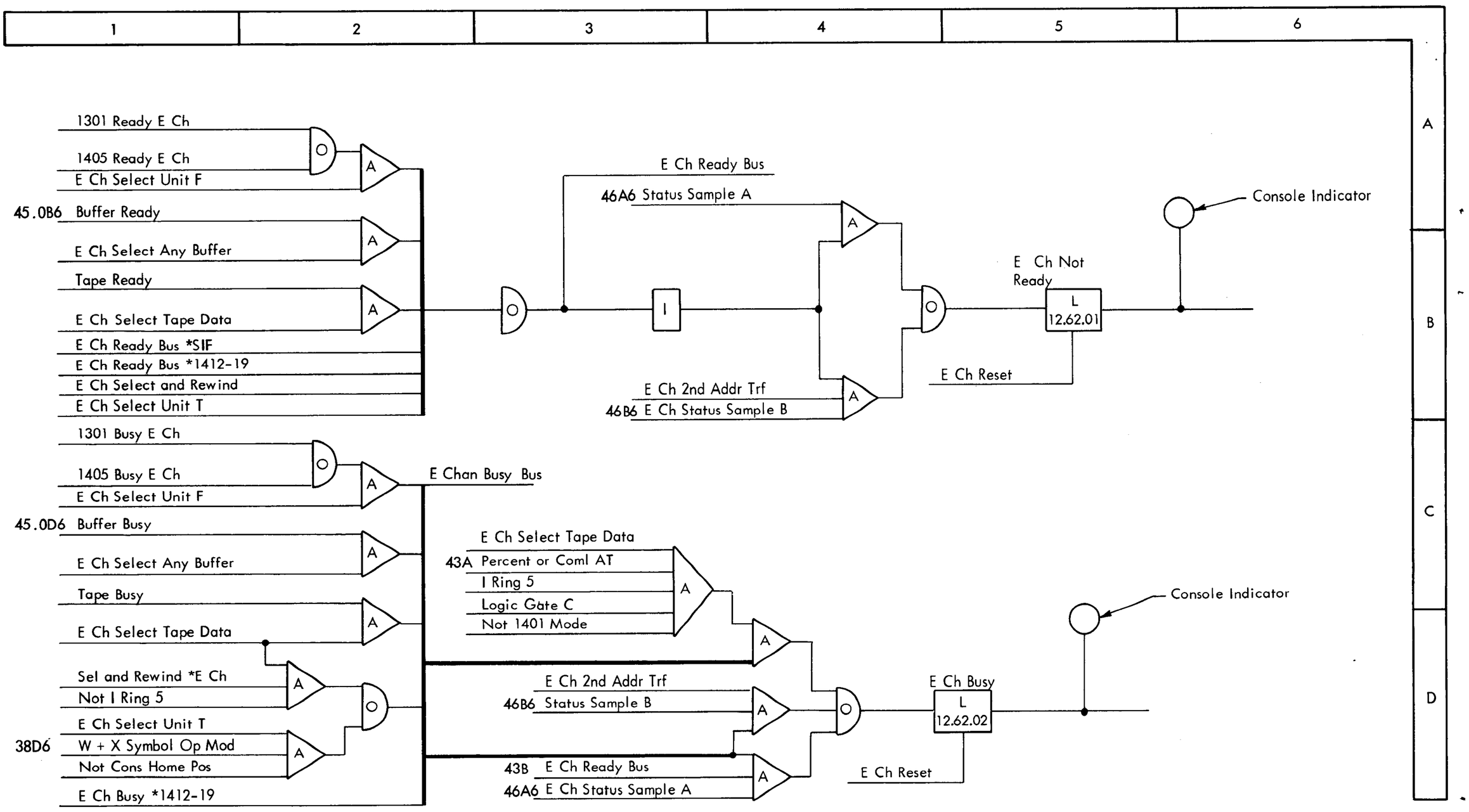


FIGURE 45.1. CHANNEL NOT READY OR BUSY

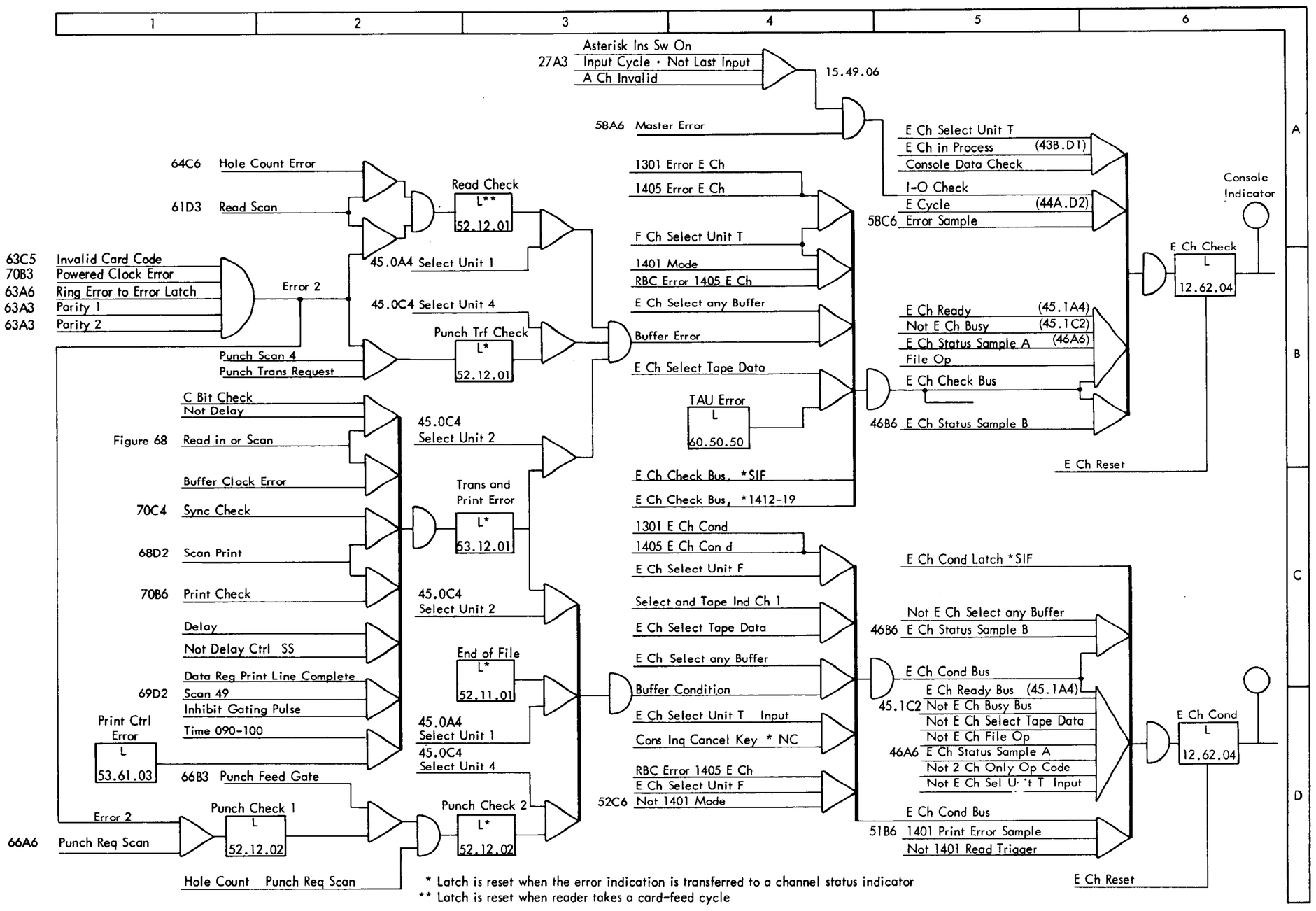


FIGURE 45.2. E CHAN CHECK AND COND

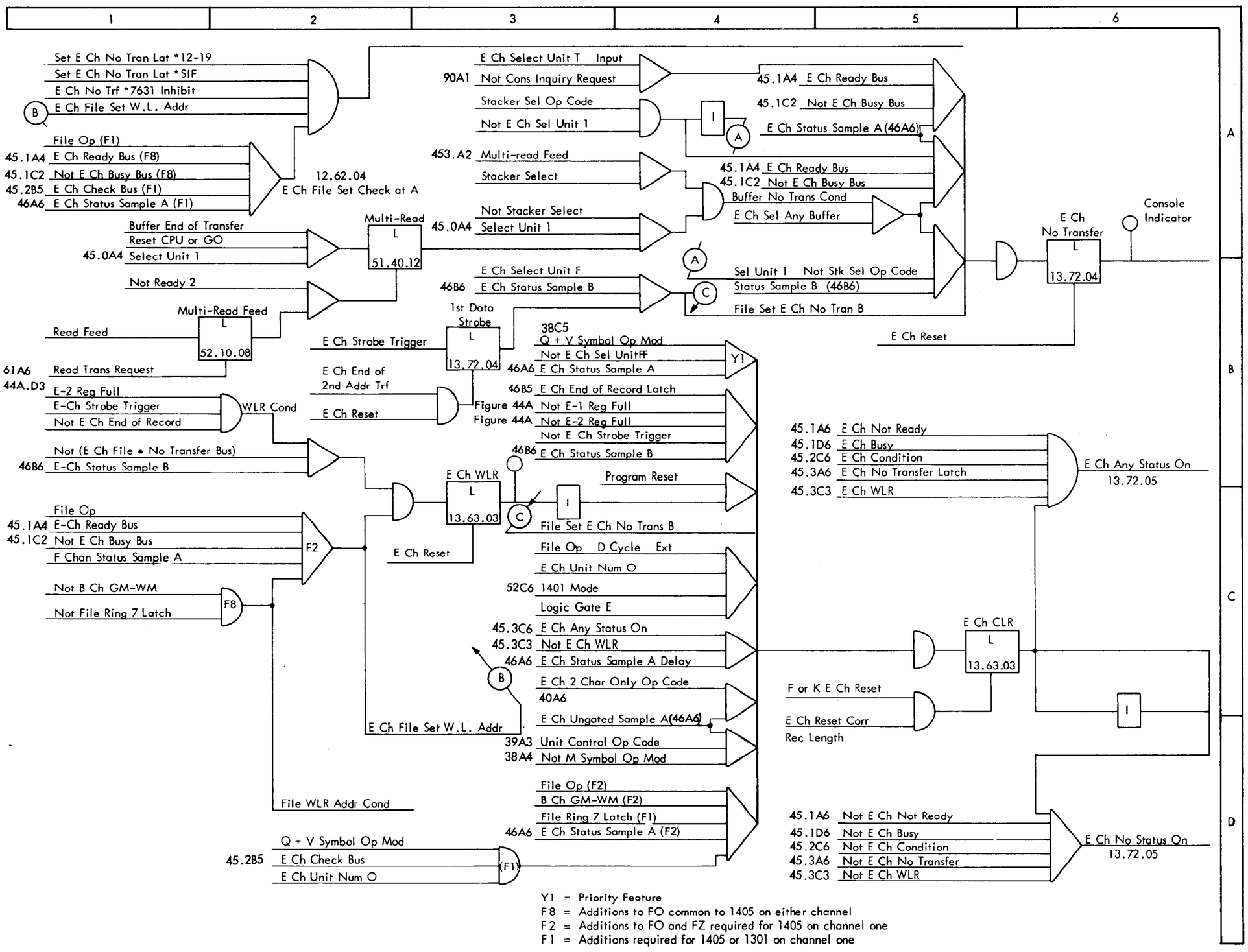


FIGURE 45.3. E CHANNEL WLR AND NO TRF

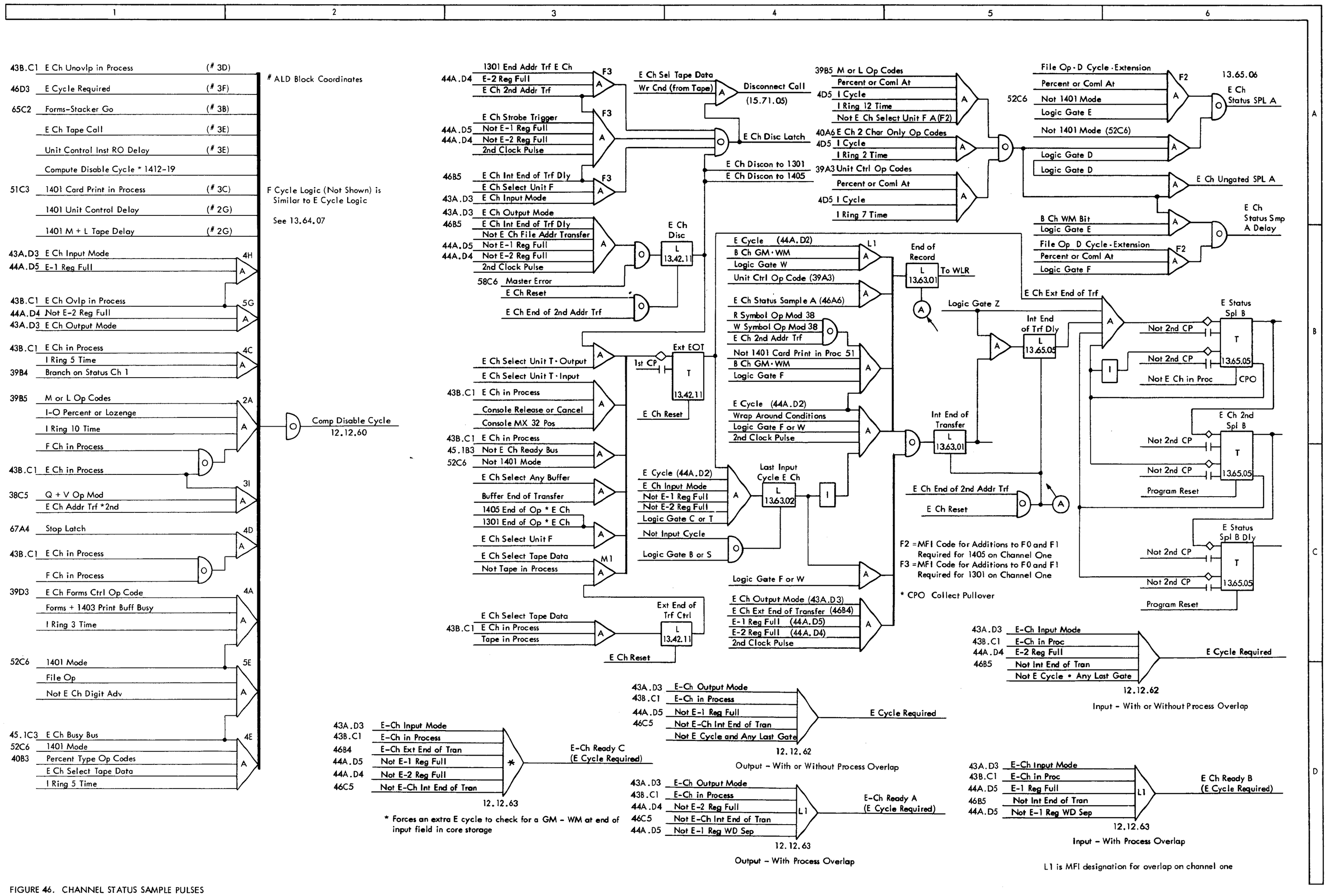
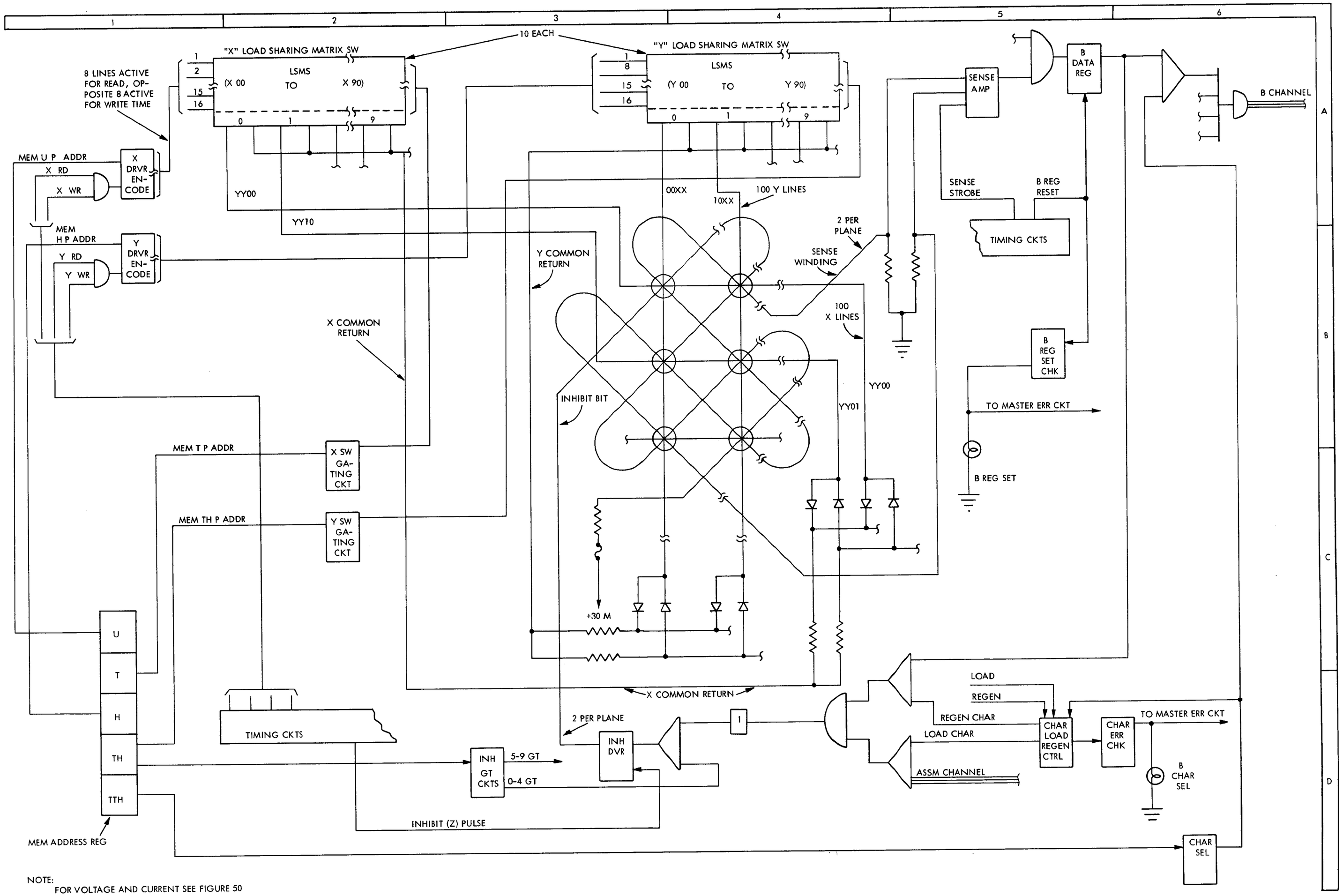
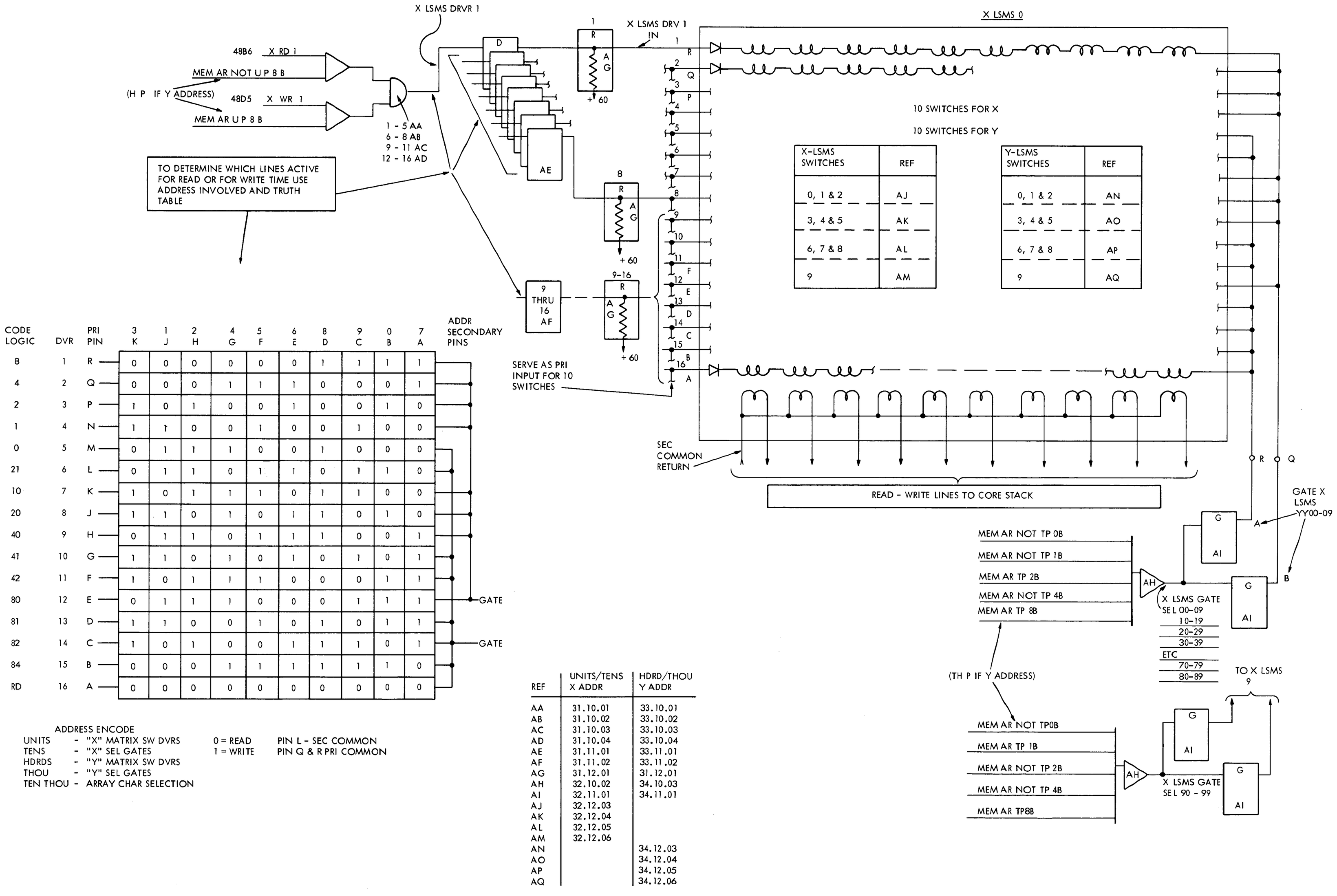


FIGURE 46. CHANNEL STATUS SAMPLE PULSES



NOTE:
FOR VOLTAGE AND CURRENT SEE FIGURE 50

FIGURE 46A. CORE STORAGE



CODE LOGIC	DVR	PRI PIN	3 K	1 J	2 H	4 G	5 F	6 E	8 D	9 C	0 B	7 A
8	1	R	0	0	0	0	0	0	1	1	1	1
4	2	Q	0	0	0	1	1	1	0	0	0	1
2	3	P	1	0	1	0	0	1	0	0	1	0
1	4	N	1	1	0	0	1	0	0	1	0	0
0	5	M	0	1	1	1	0	0	1	0	0	0
21	6	L	0	1	1	0	1	1	0	1	1	0
10	7	K	1	0	1	1	1	0	1	1	0	0
20	8	J	1	1	0	1	0	1	1	0	1	0
40	9	H	0	1	1	0	1	1	1	0	0	1
41	10	G	1	1	0	1	0	1	0	1	0	1
42	11	F	1	0	1	1	1	0	0	0	1	1
80	12	E	0	1	1	1	0	0	0	1	1	1
81	13	D	1	1	0	0	1	0	1	0	1	1
82	14	C	1	0	1	0	0	1	1	1	0	1
84	15	B	0	0	0	1	1	1	1	1	1	0
RD	16	A	0	0	0	0	0	0	0	0	0	0

ADDR SECONDARY PINS

GATE

GATE

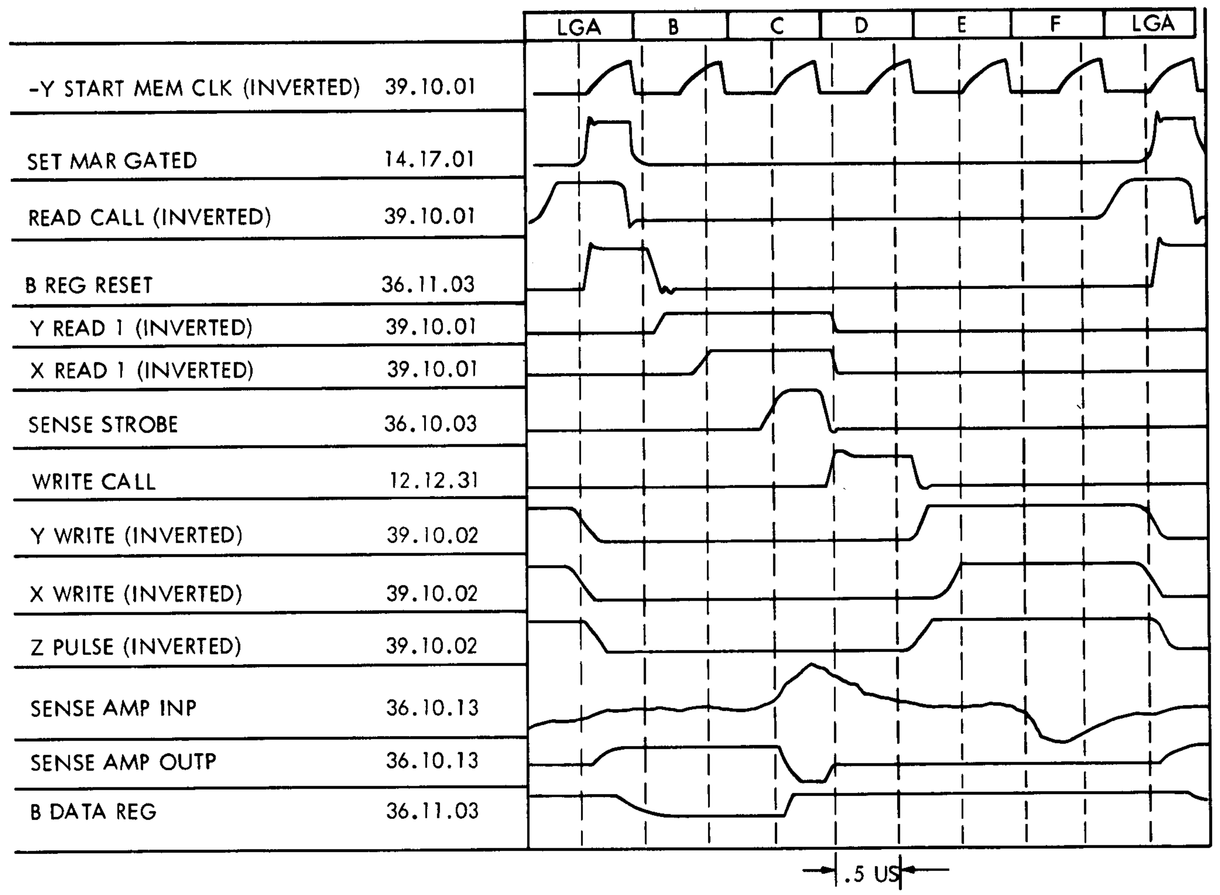
ADDRESS ENCODE
UNITS - "X" MATRIX SW DVRS
TENS - "X" SEL GATES
HDRDS - "Y" MATRIX SW DVRS
THOU - "Y" SEL GATES
TEN THOU - ARRAY CHAR SELECTION

0 = READ
1 = WRITE

PIN L - SEC COMMON
PIN Q & R PRI COMMON

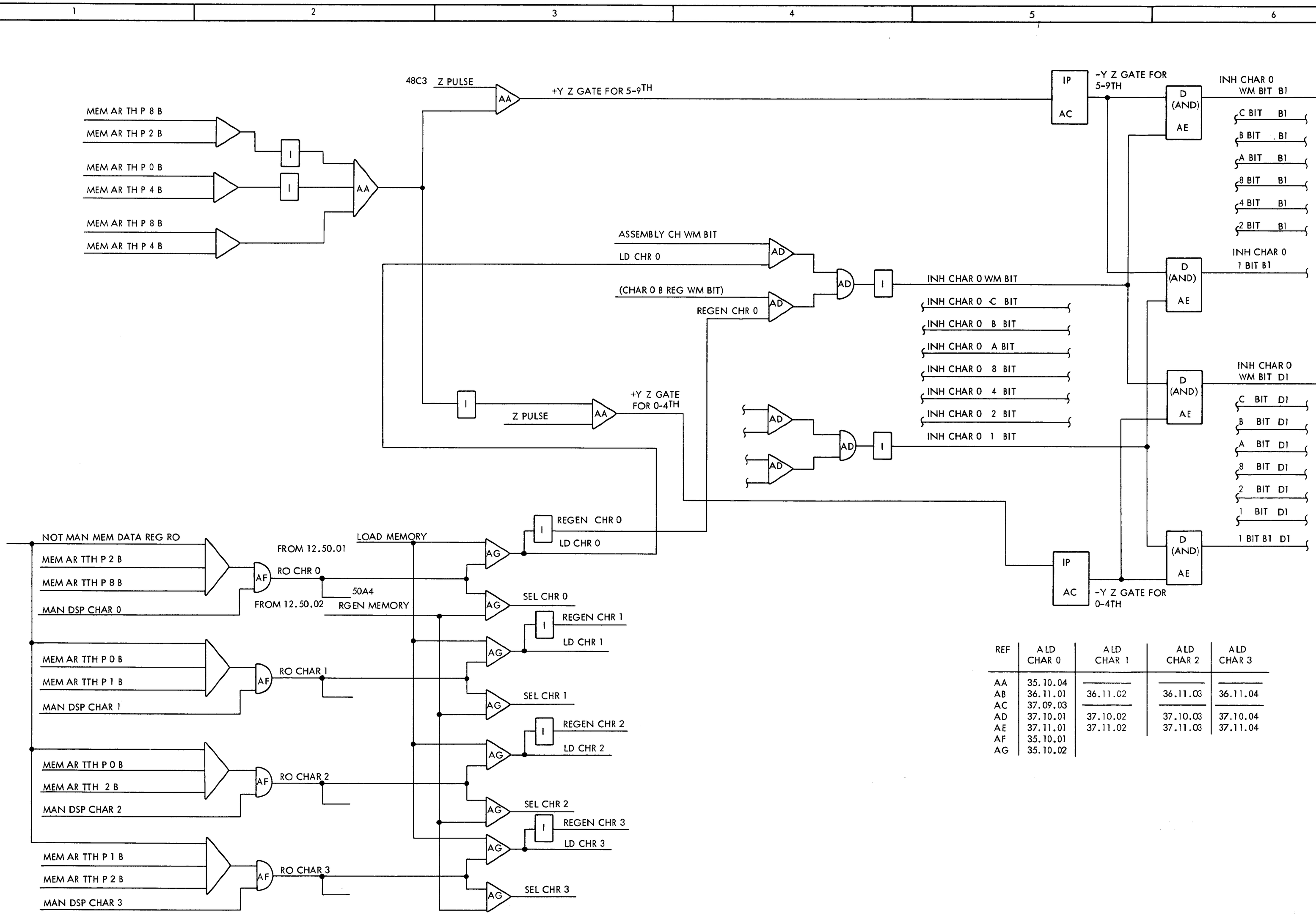
REF	UNITS/TENS X ADDR	HDRD/THOU Y ADDR
AA	31.10.01	33.10.01
AB	31.10.02	33.10.02
AC	31.10.03	33.10.03
AD	31.10.04	33.10.04
AE	31.11.01	33.11.01
AF	31.11.02	33.11.02
AG	31.12.01	31.12.01
AH	32.10.02	34.10.03
AI	32.11.01	34.11.01
AJ	32.12.03	
AK	32.12.04	
AL	32.12.05	
AM	32.12.06	
AN		34.12.03
AO		34.12.04
AP		34.12.05
AQ		34.12.06

FIGURE 47. LSMS, PRI DRVRS, & GATE SEL



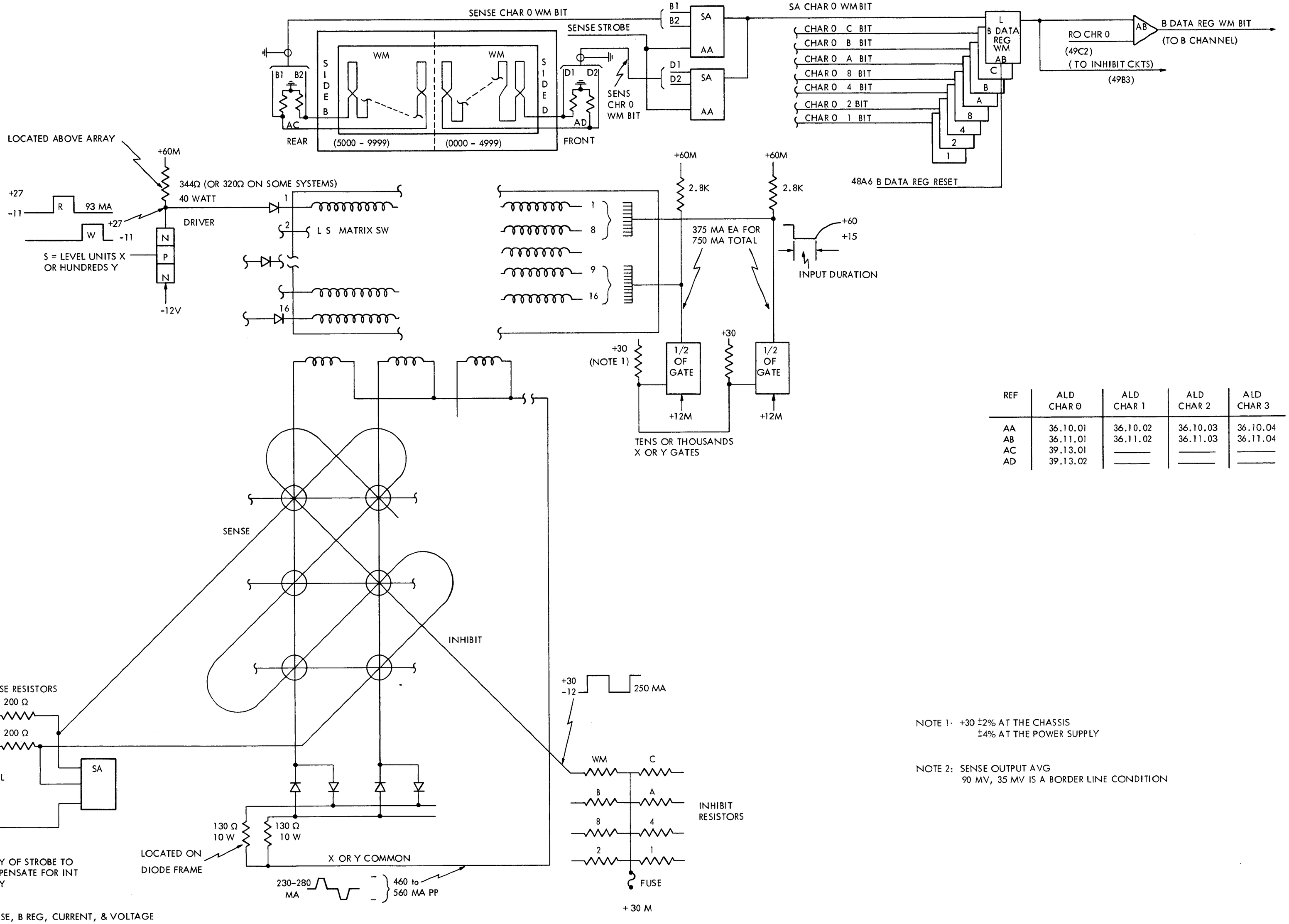
REF	ALD
AA	14.71.51
AB	39.10.01
AC	39.10.02
AD	39.10.03

FIGURE 48. MEM CLOCK TIMING



REF	ALD CHAR 0	ALD CHAR 1	ALD CHAR 2	ALD CHAR 3
AA	35.10.04			
AB	36.11.01	36.11.02	36.11.03	36.11.04
AC	37.09.03			
AD	37.10.01	37.10.02	37.10.03	37.10.04
AE	37.11.01	37.11.02	37.11.03	37.11.04
AF	35.10.01			
AG	35.10.02			

FIGURE 49. INHIBIT, LOAD, REGEN CTRLS



REF	ALD CHAR 0	ALD CHAR 1	ALD CHAR 2	ALD CHAR 3
AA	36.10.01	36.10.02	36.10.03	36.10.04
AB	36.11.01	36.11.02	36.11.03	36.11.04
AC	39.13.01	———	———	———
AD	39.13.02	———	———	———

NOTE 1: +30 ±2% AT THE CHASSIS
±4% AT THE POWER SUPPLY

NOTE 2: SENSE OUTPUT AVG
90 MV, 35 MV IS A BORDER LINE CONDITION

FIGURE 50. SENSE, B REG, CURRENT, & VOLTAGE

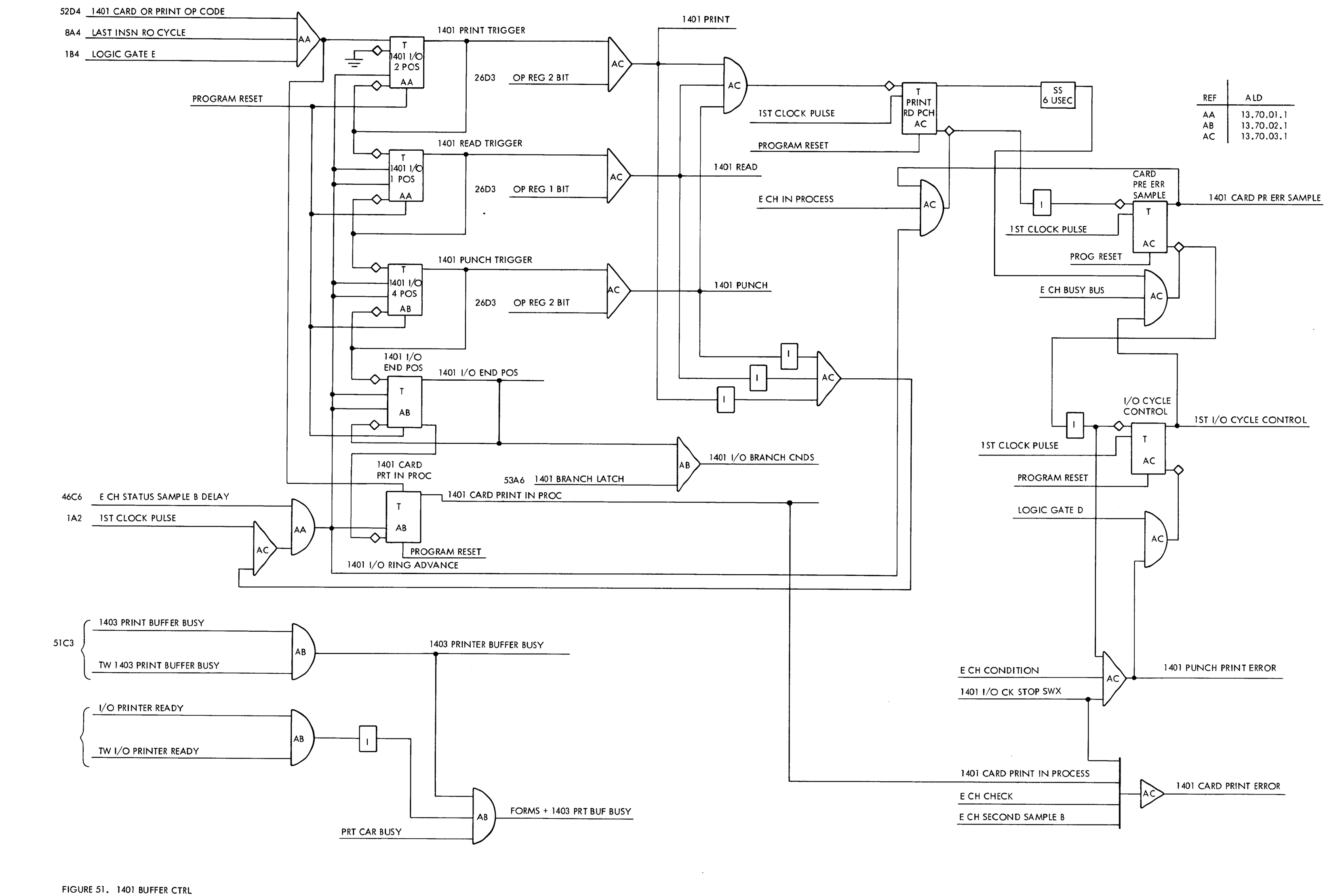
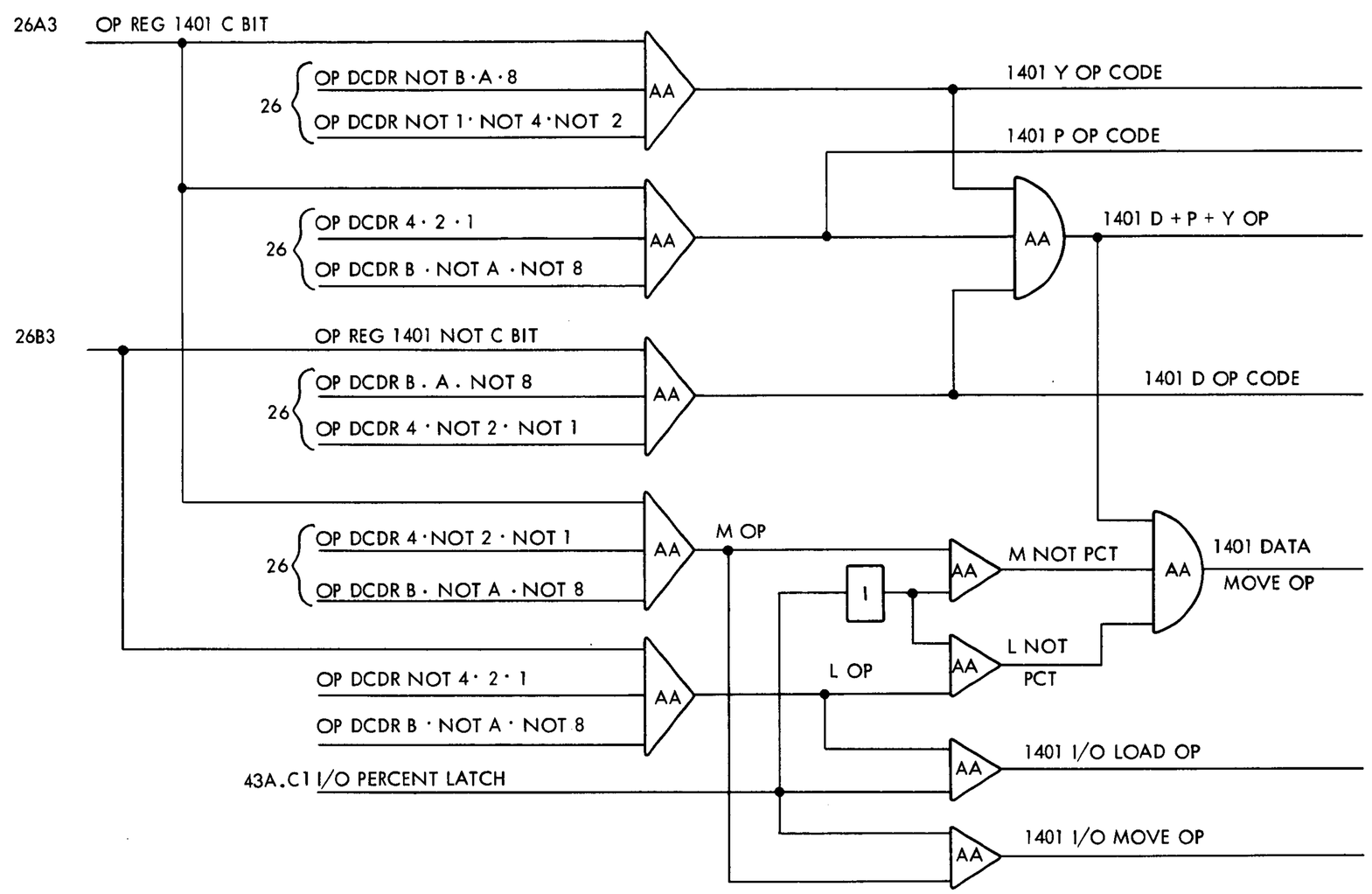
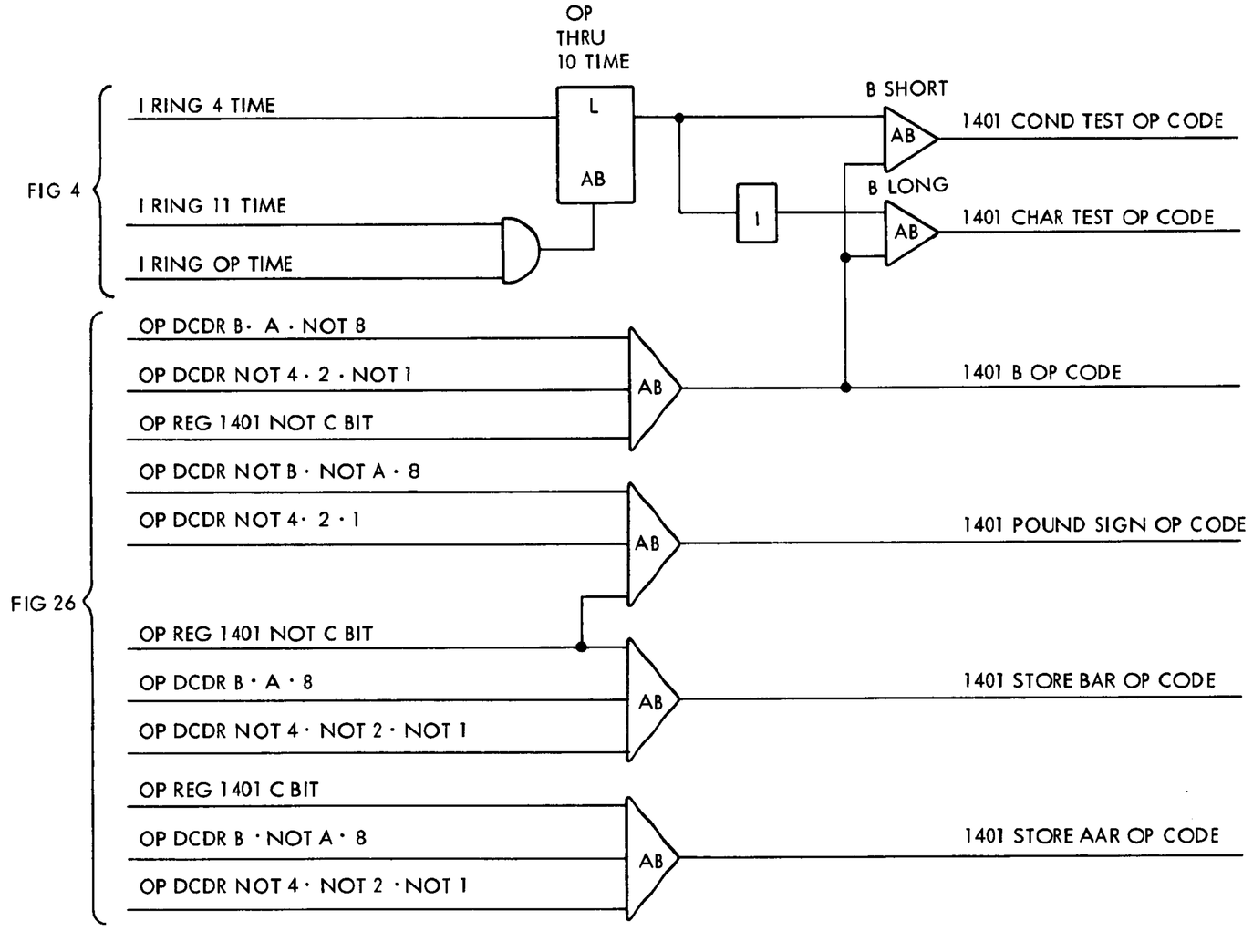
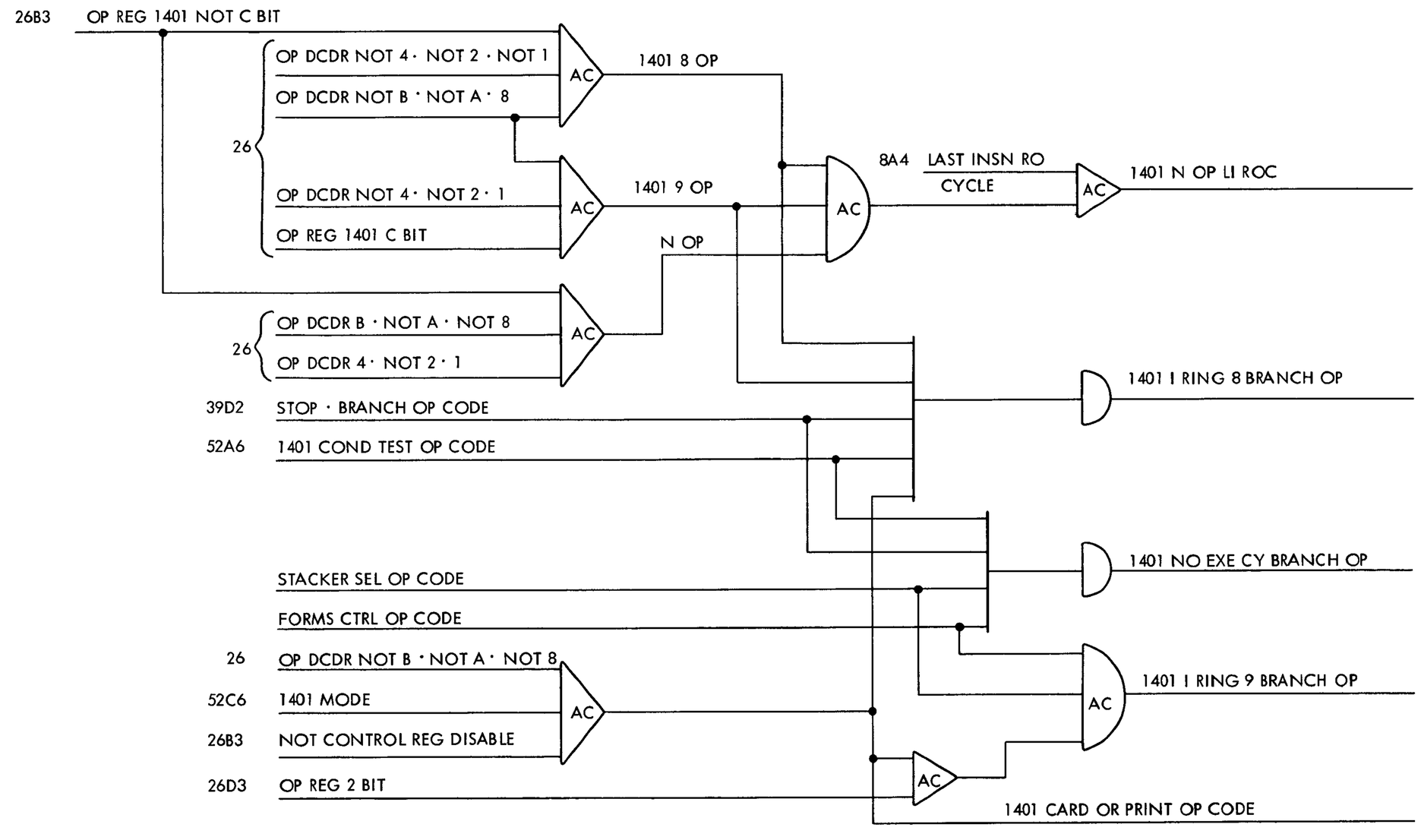
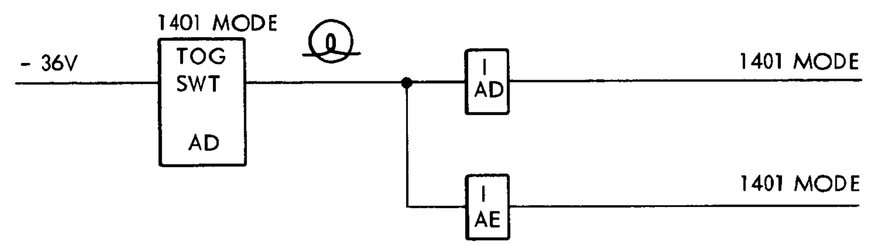


FIGURE 51. 1401 BUFFER CTRL









REF	ALD
AA	13.13.09.1
AB	13.13.10.1
AC	13.13.11.1
AD	12.65.10.1
AE	12.65.11.1

FIGURE 52. 1401 OP DECODE

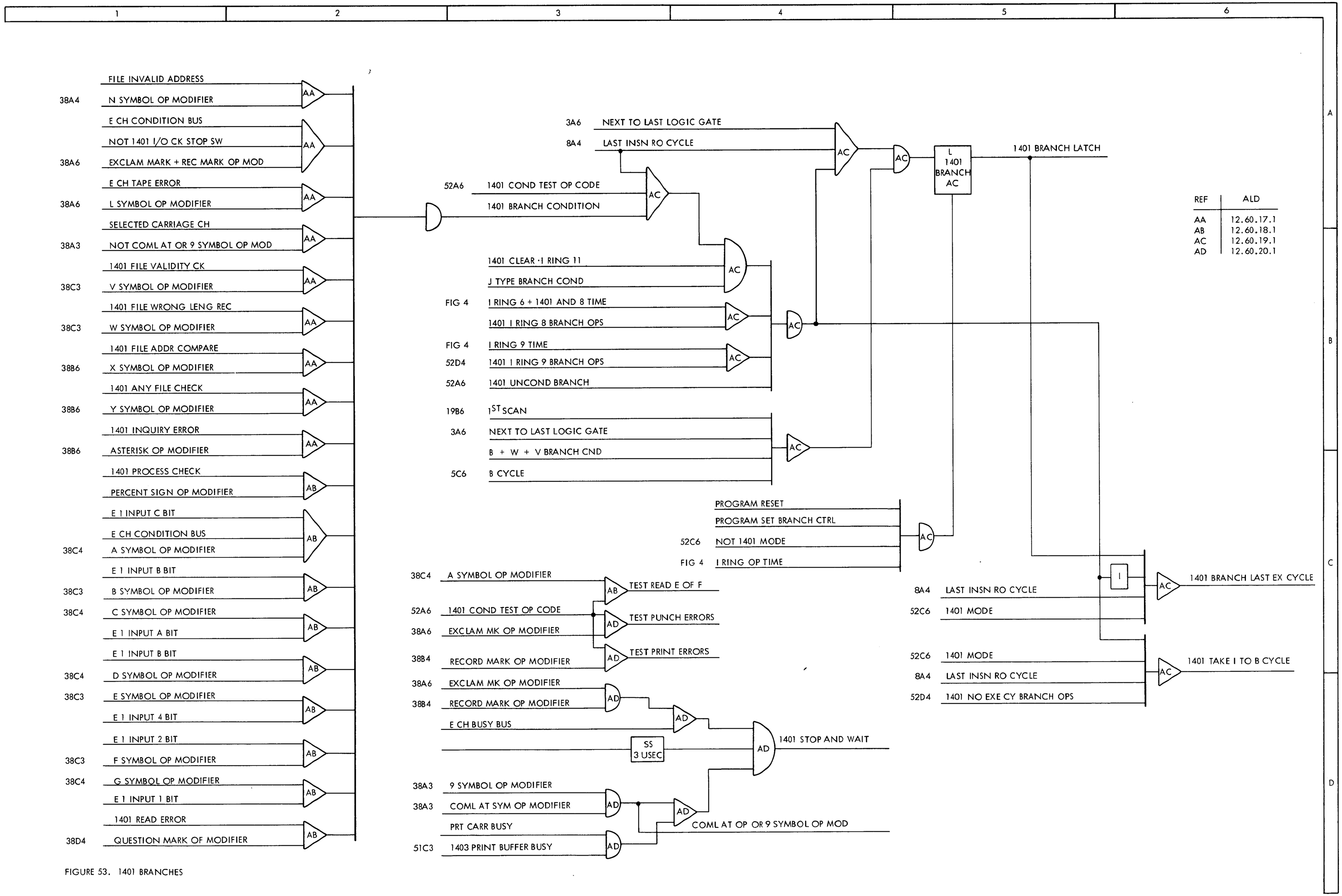


FIGURE 53. 1401 BRANCHES

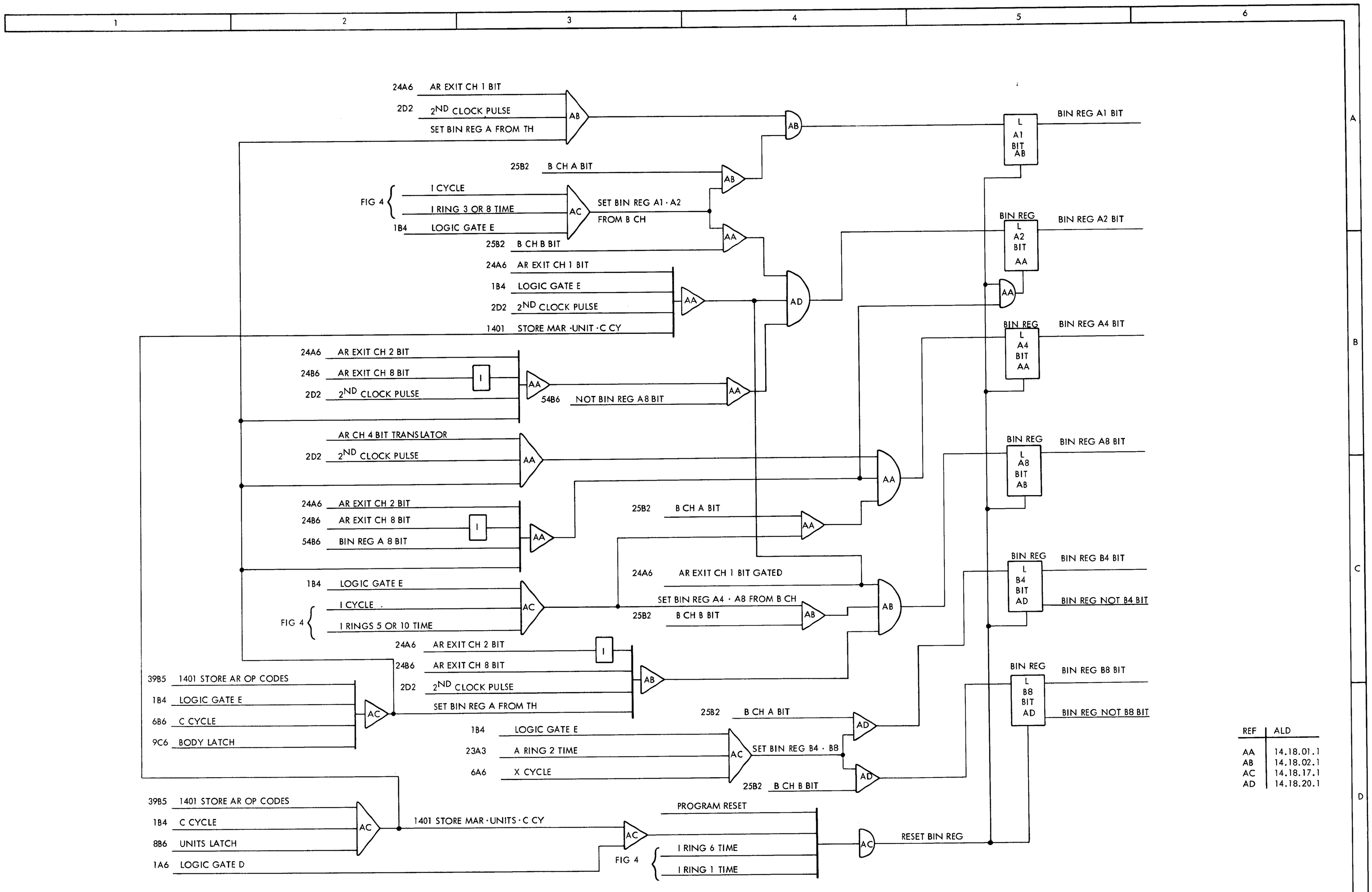


FIGURE 54. BIN REG & SET CTRL

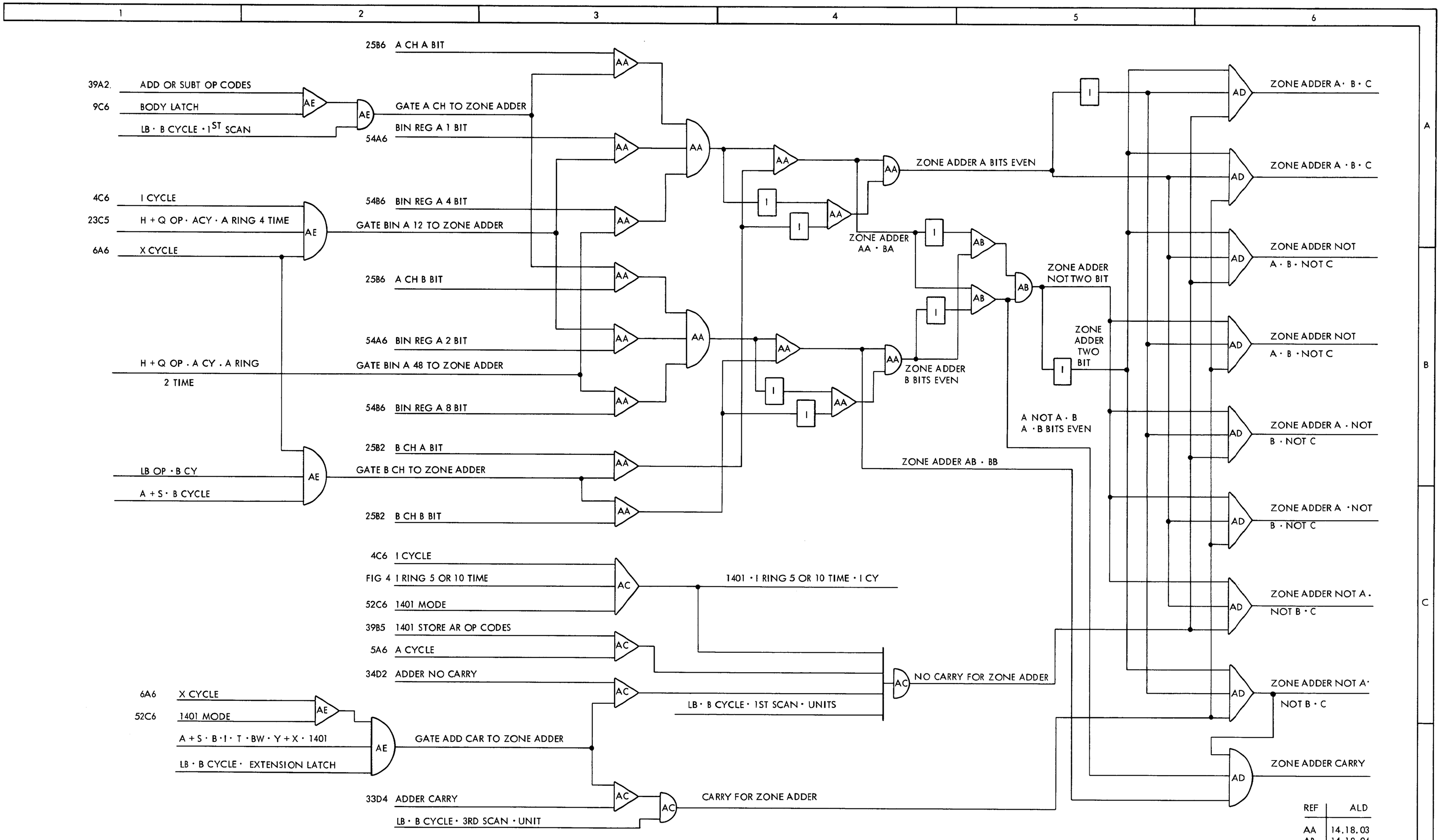


FIGURE 55. ZONE ADDER

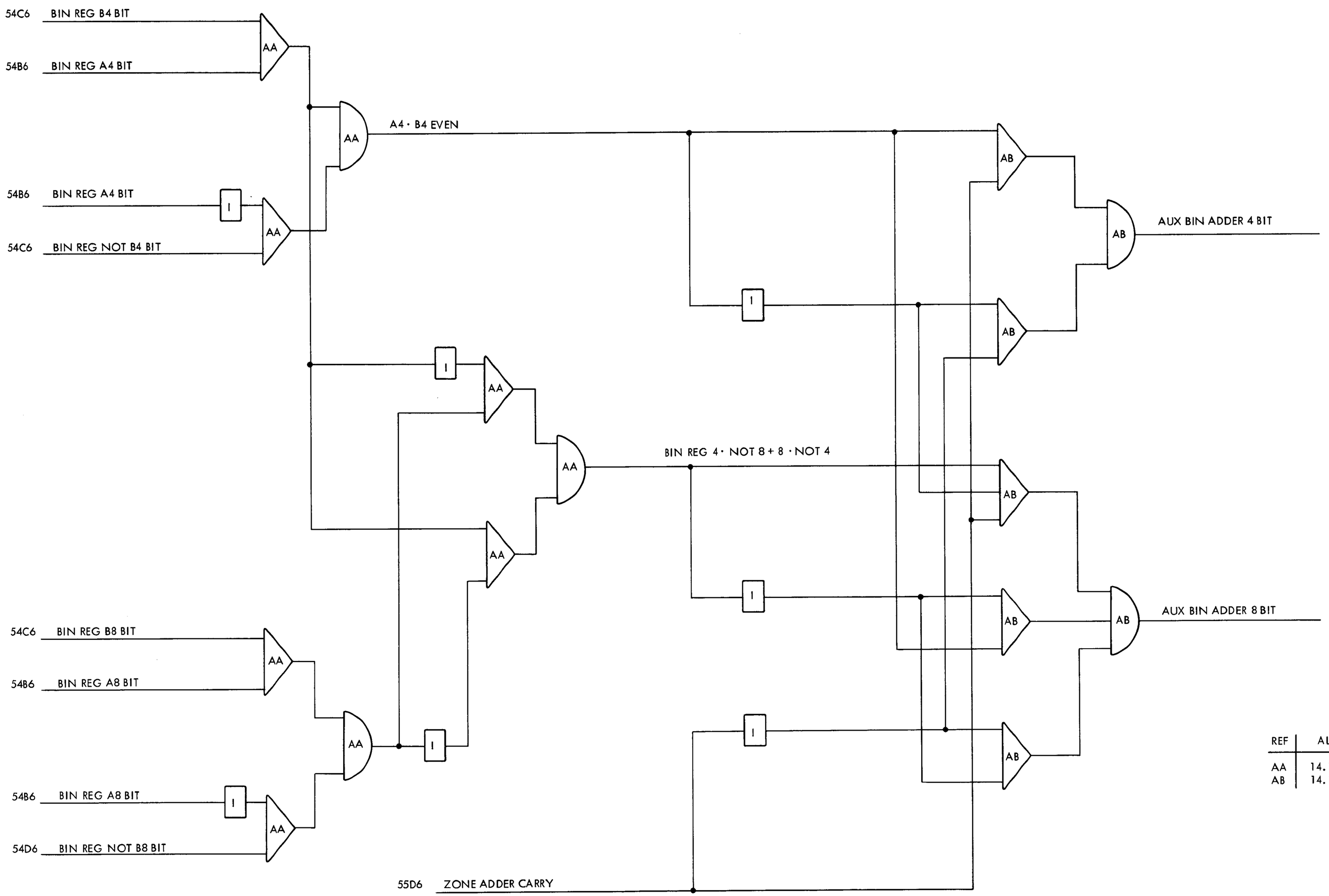
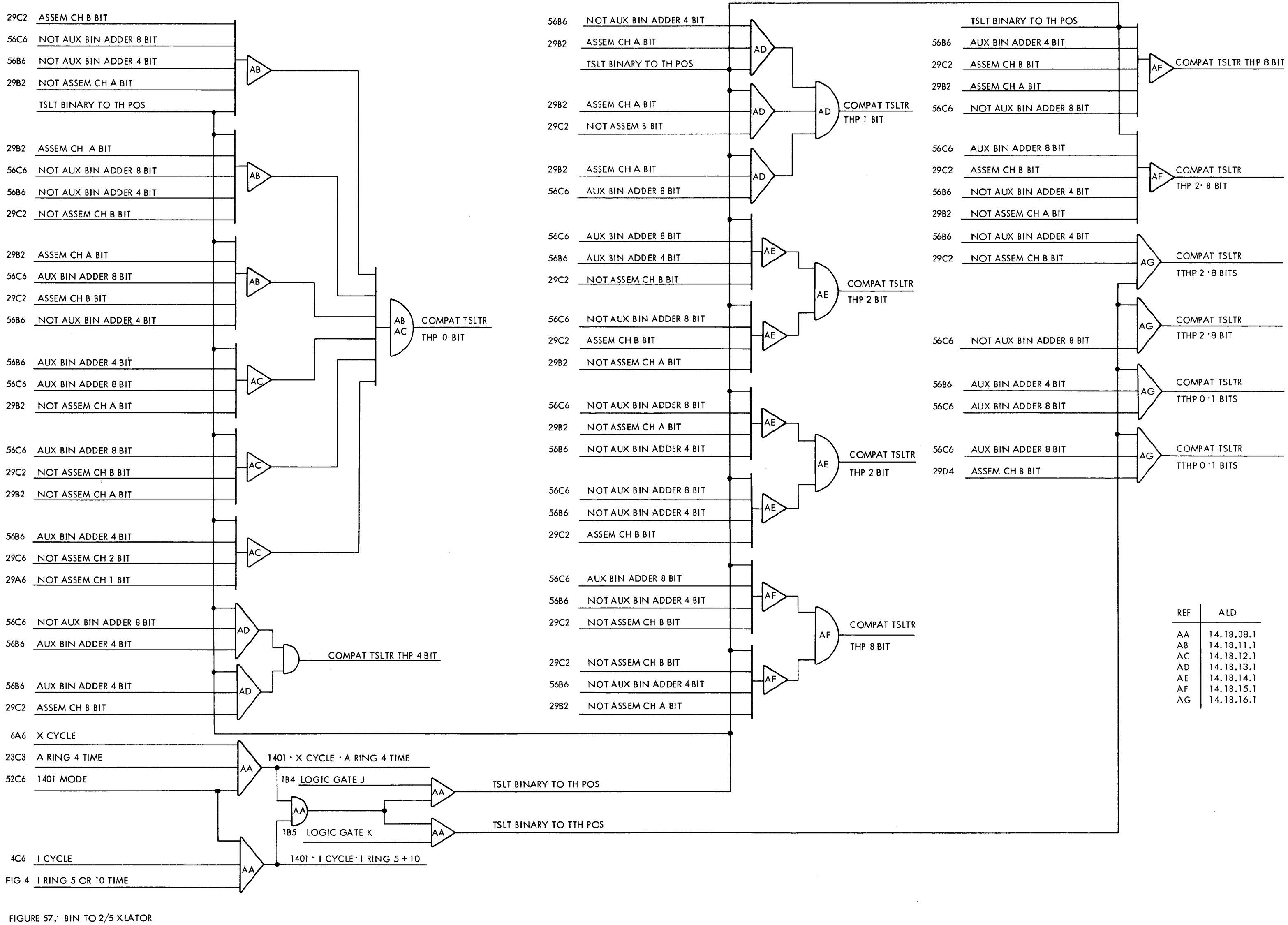


FIGURE 56. AUX BIN ADDER



REF	ALD
AA	14.18.08.1
AB	14.18.11.1
AC	14.18.12.1
AD	14.18.13.1
AE	14.18.14.1
AF	14.18.15.1
AG	14.18.16.1

FIGURE 57. BIN TO 2/5 XLATOR

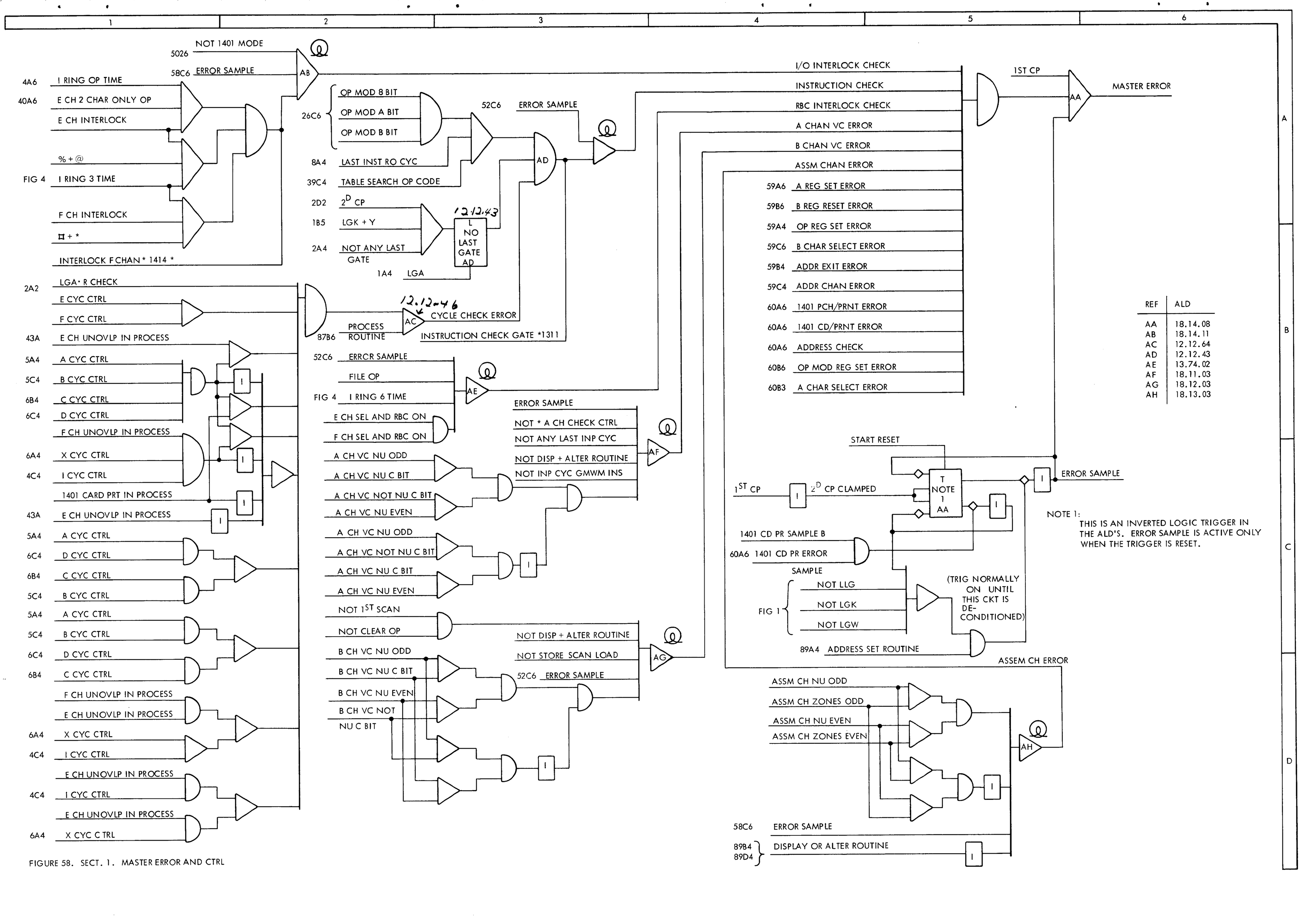
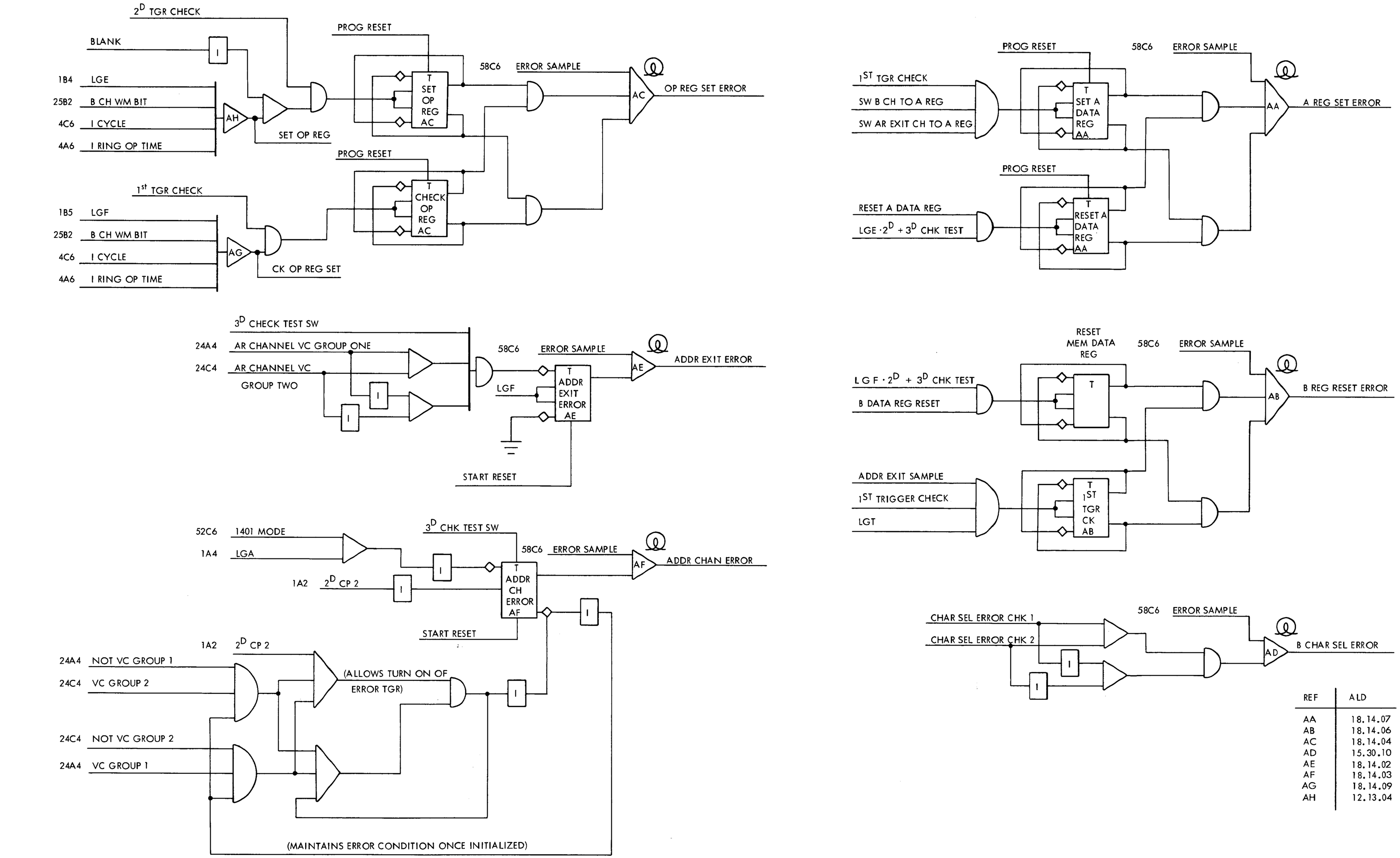


FIGURE 58. SECT. 1. MASTER ERROR AND CTRL



REF	ALD
AA	18.14.07
AB	18.14.06
AC	18.14.04
AD	15.30.10
AE	18.14.02
AF	18.14.03
AG	18.14.09
AH	12.13.04

FIGURE 59. SECT 2 MASTER ERROR & CTRL

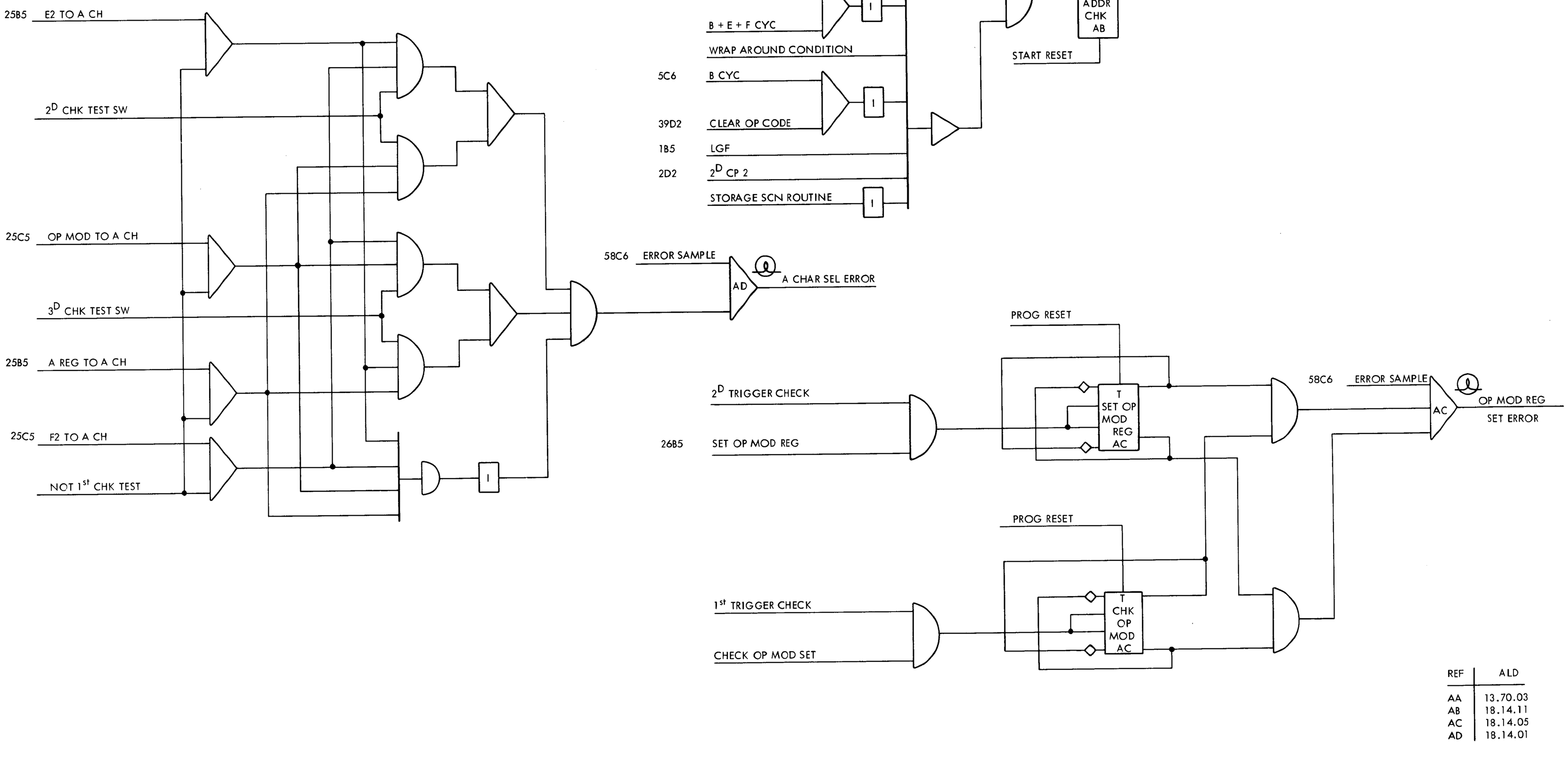
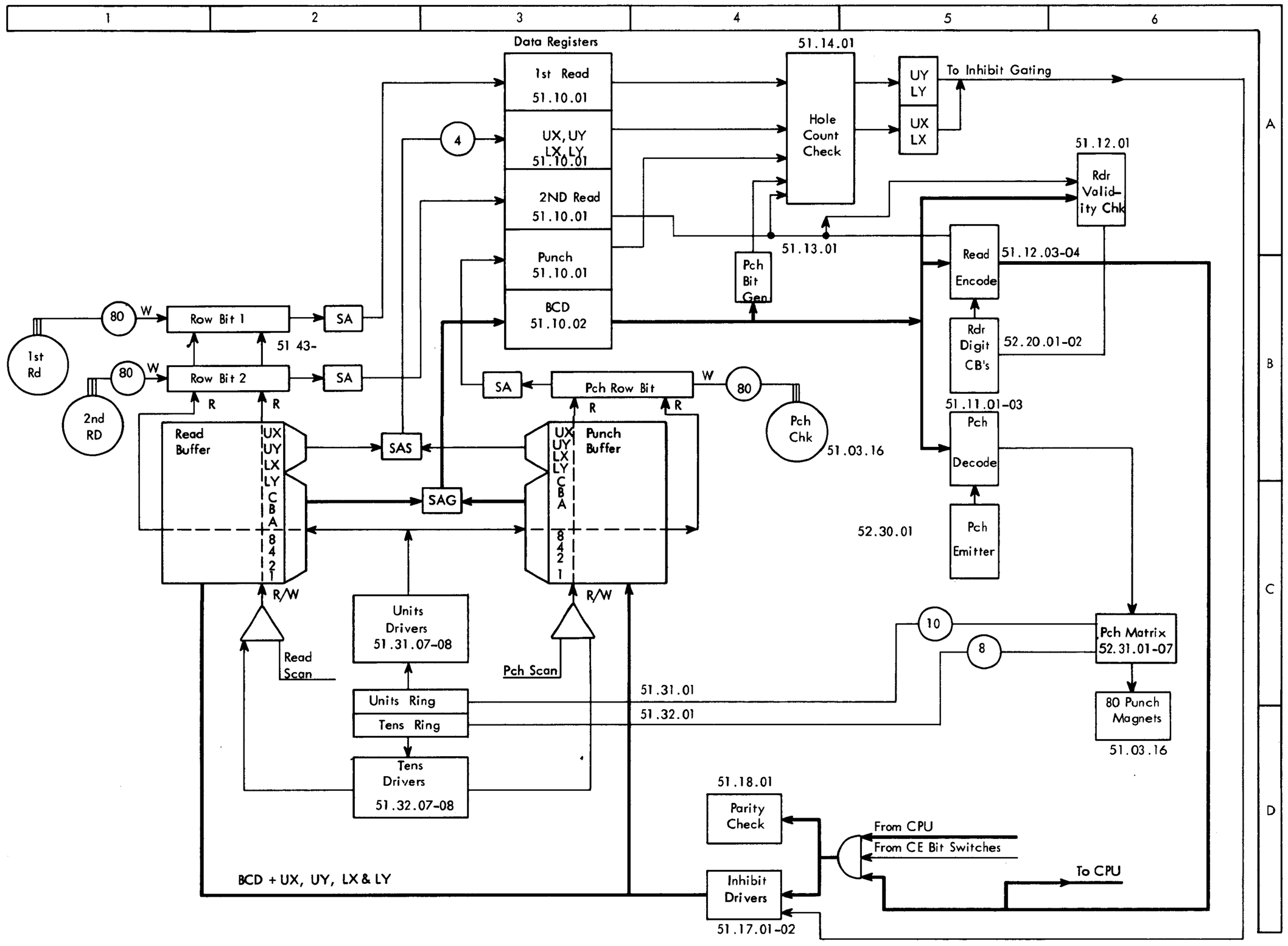


FIGURE 60. SECT 3 MASTER ERROR & CTRL



(Heavy Line is BCD)

FIGURE 61A. INT BFR DATA FLOW

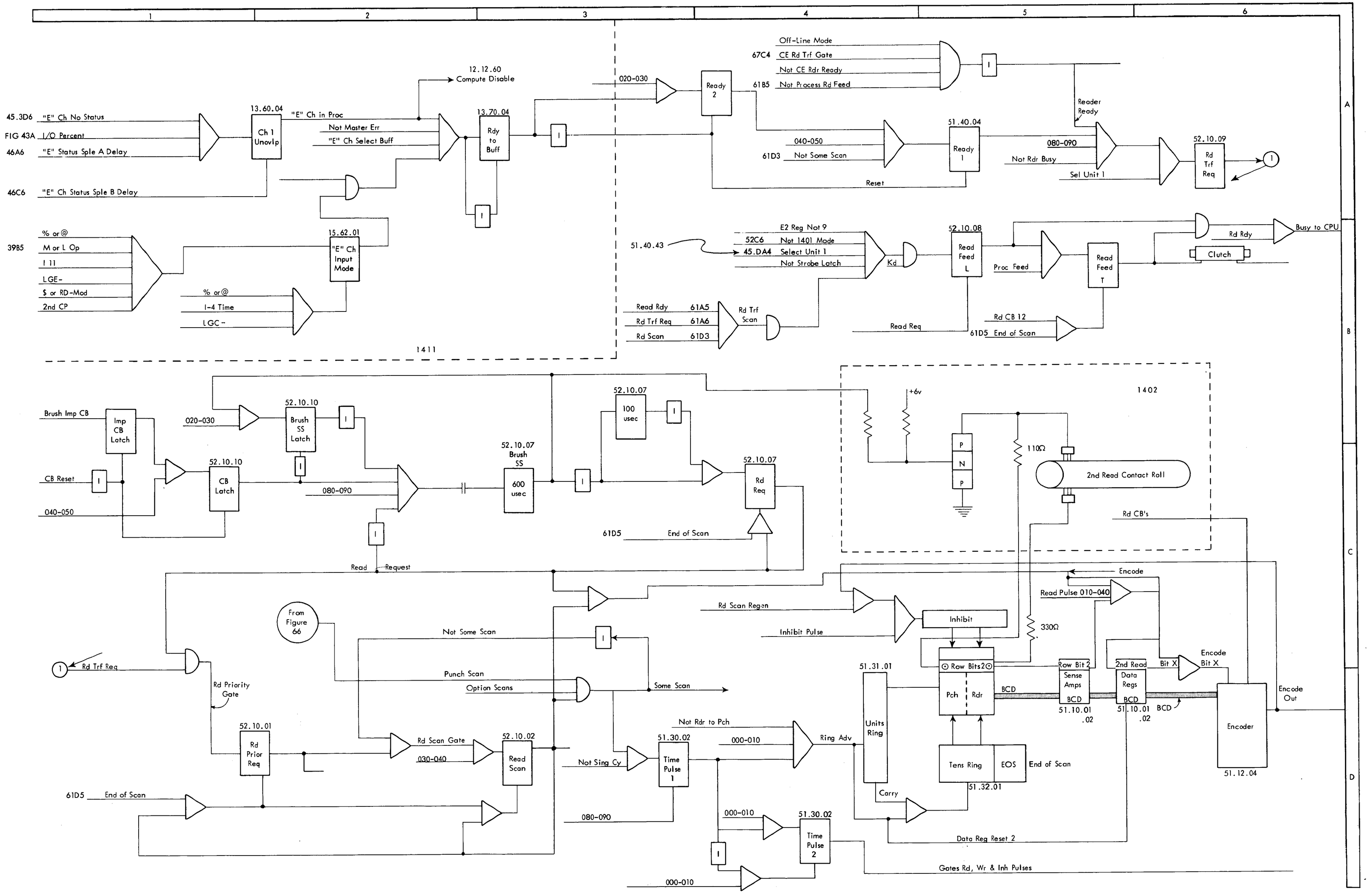
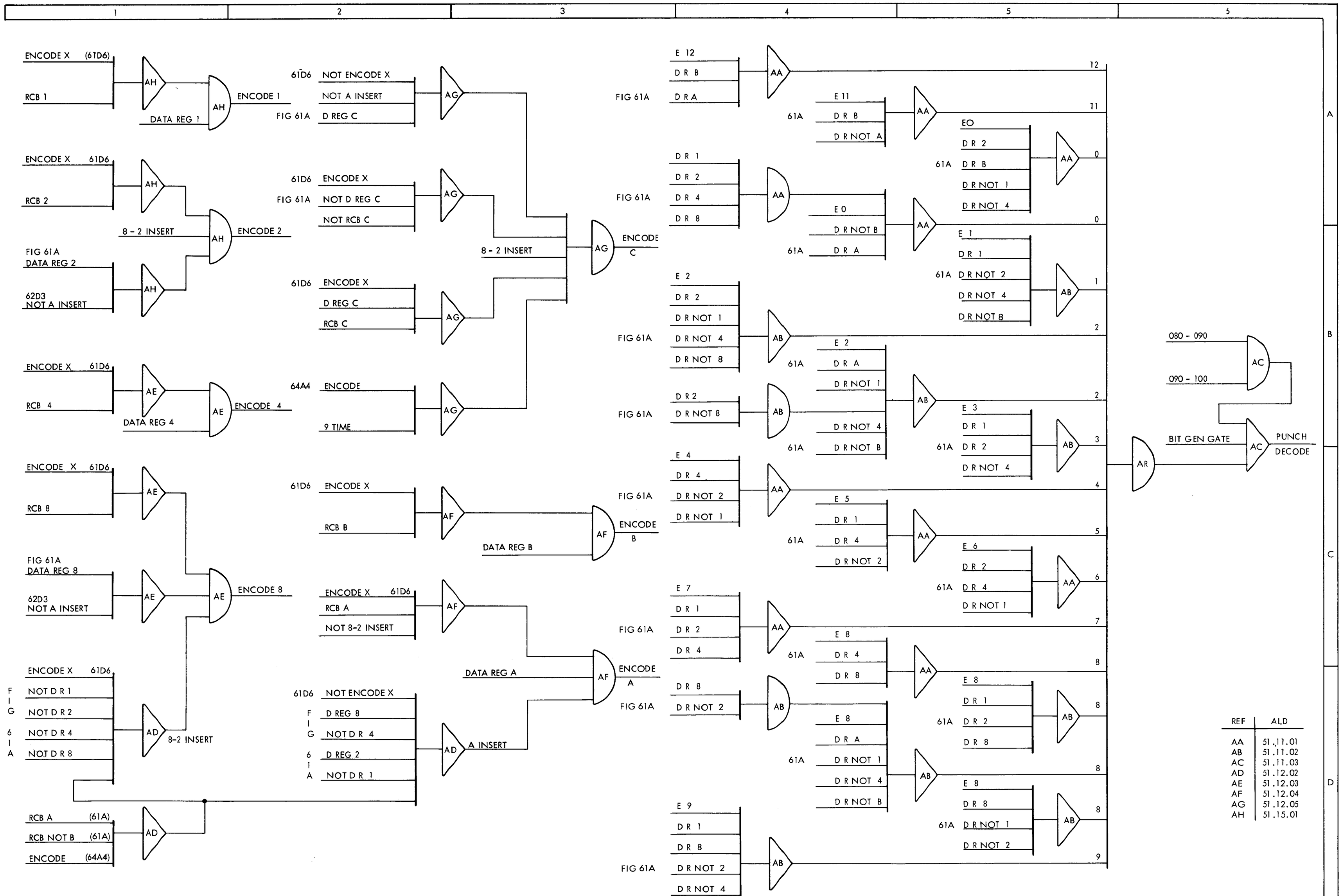
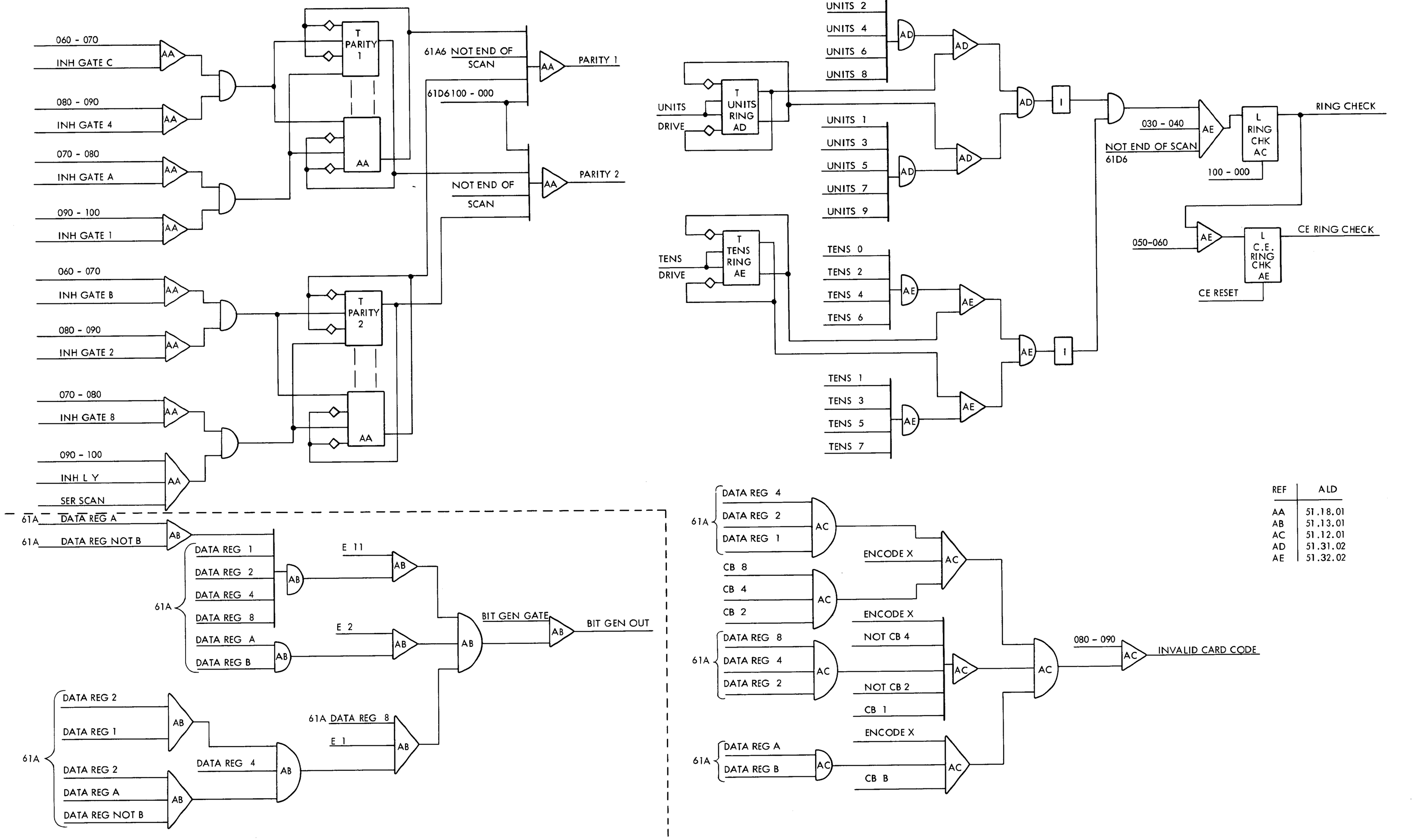


FIGURE 61. READER CONTROL



REF	ALD
AA	51.11.01
AB	51.11.02
AC	51.11.03
AD	51.12.02
AE	51.12.03
AF	51.12.04
AG	51.12.05
AH	51.15.01

FIGURE 62. RD ENCODE AND PCH DECODE



REF	ALD
AA	51.18.01
AB	51.13.01
AC	51.12.01
AD	51.31.02
AE	51.32.02

FIGURE 63. INT BUFFER CHECKS AND PUNCH BIT GENERATE

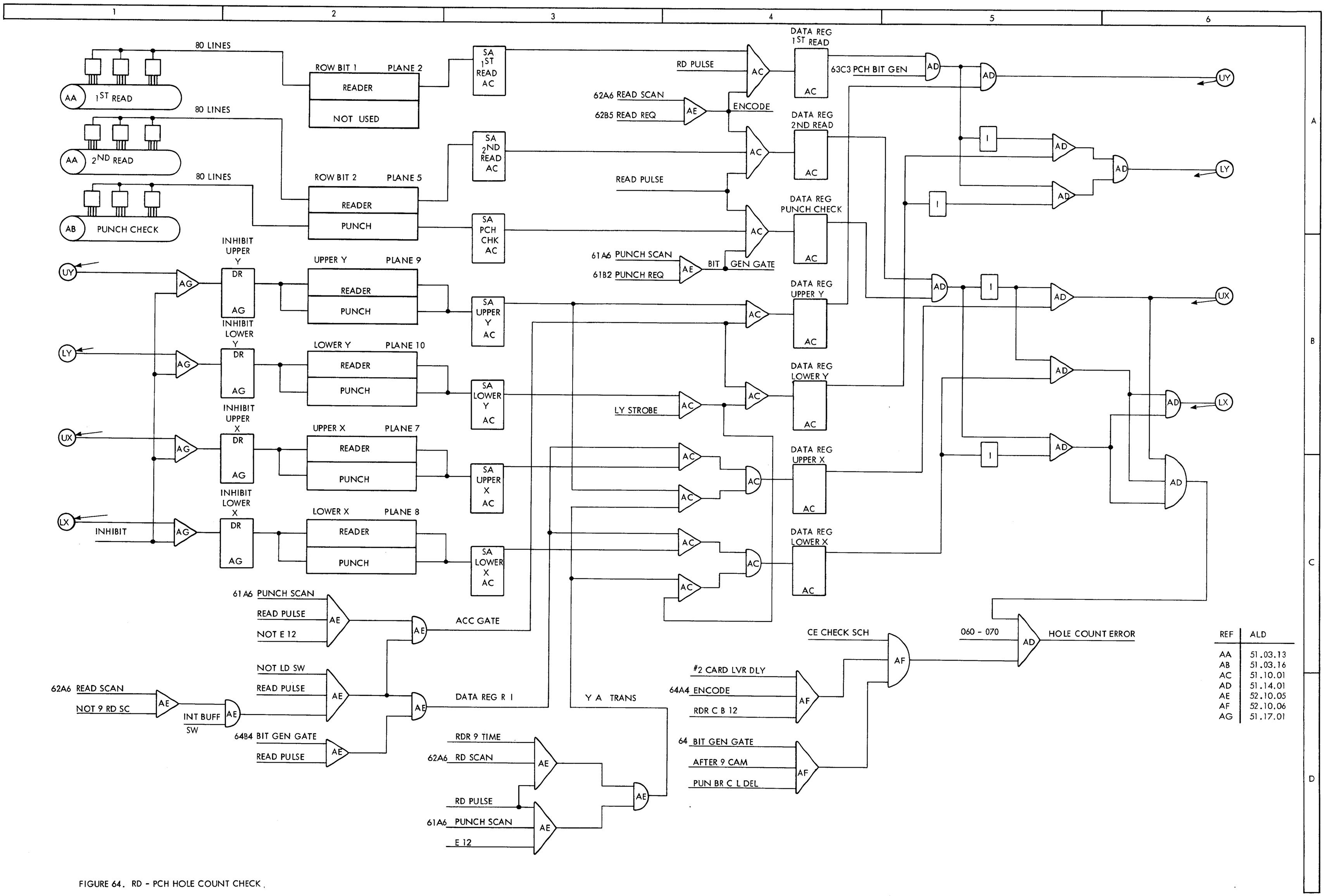


FIGURE 64. RD - PCH HOLE COUNT CHECK.

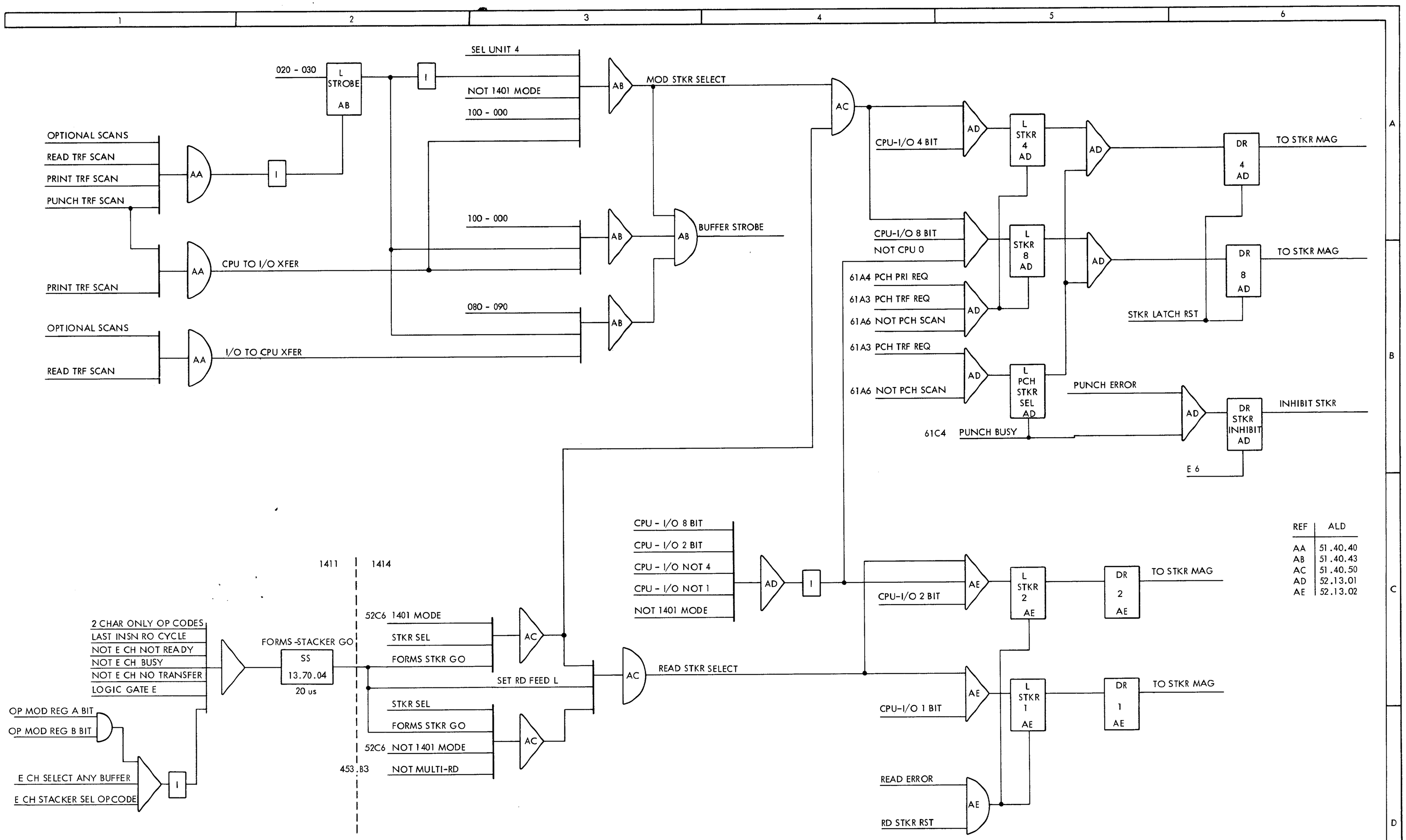


FIGURE 65. BUFFER STROBE AND STACK SEL

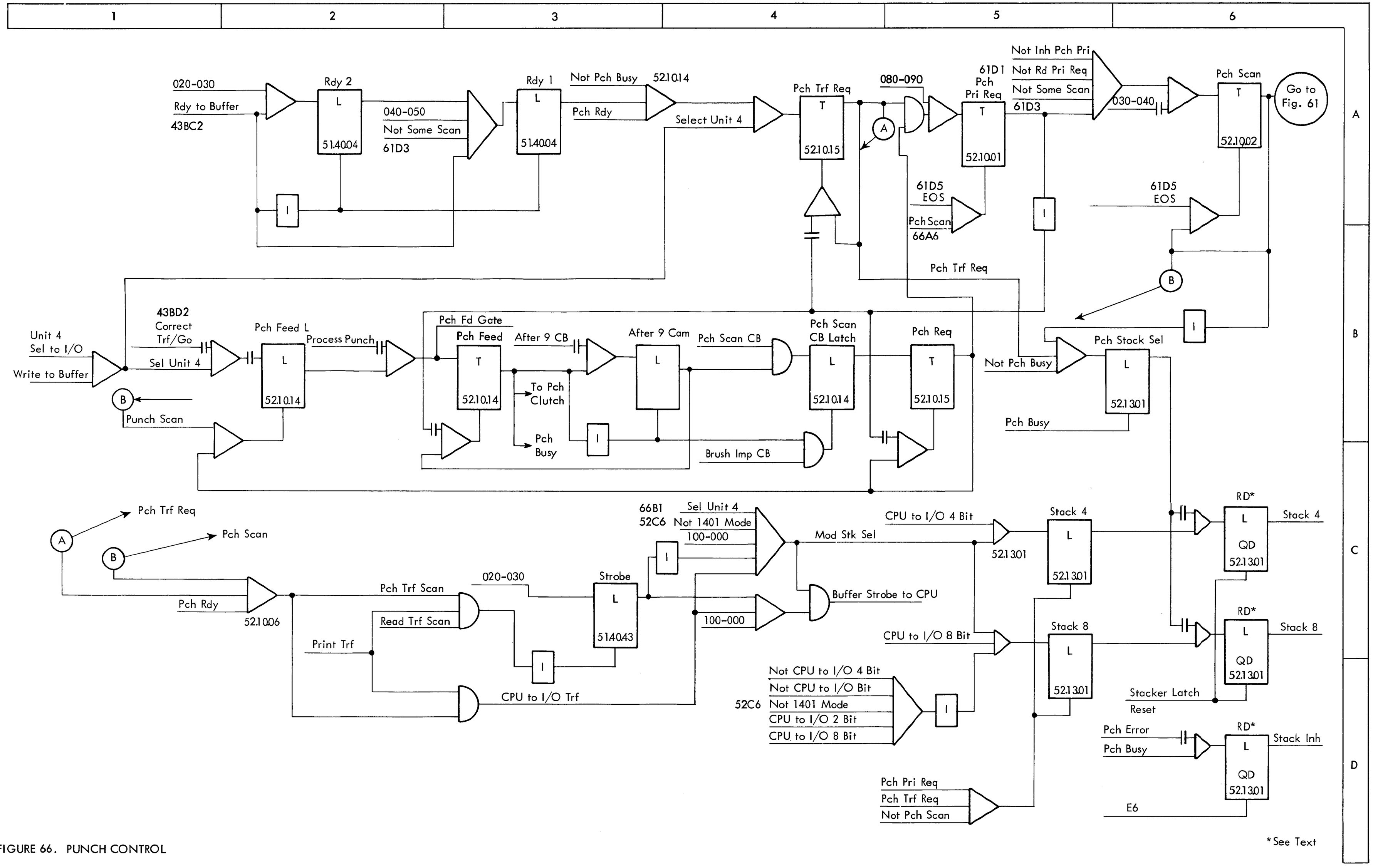
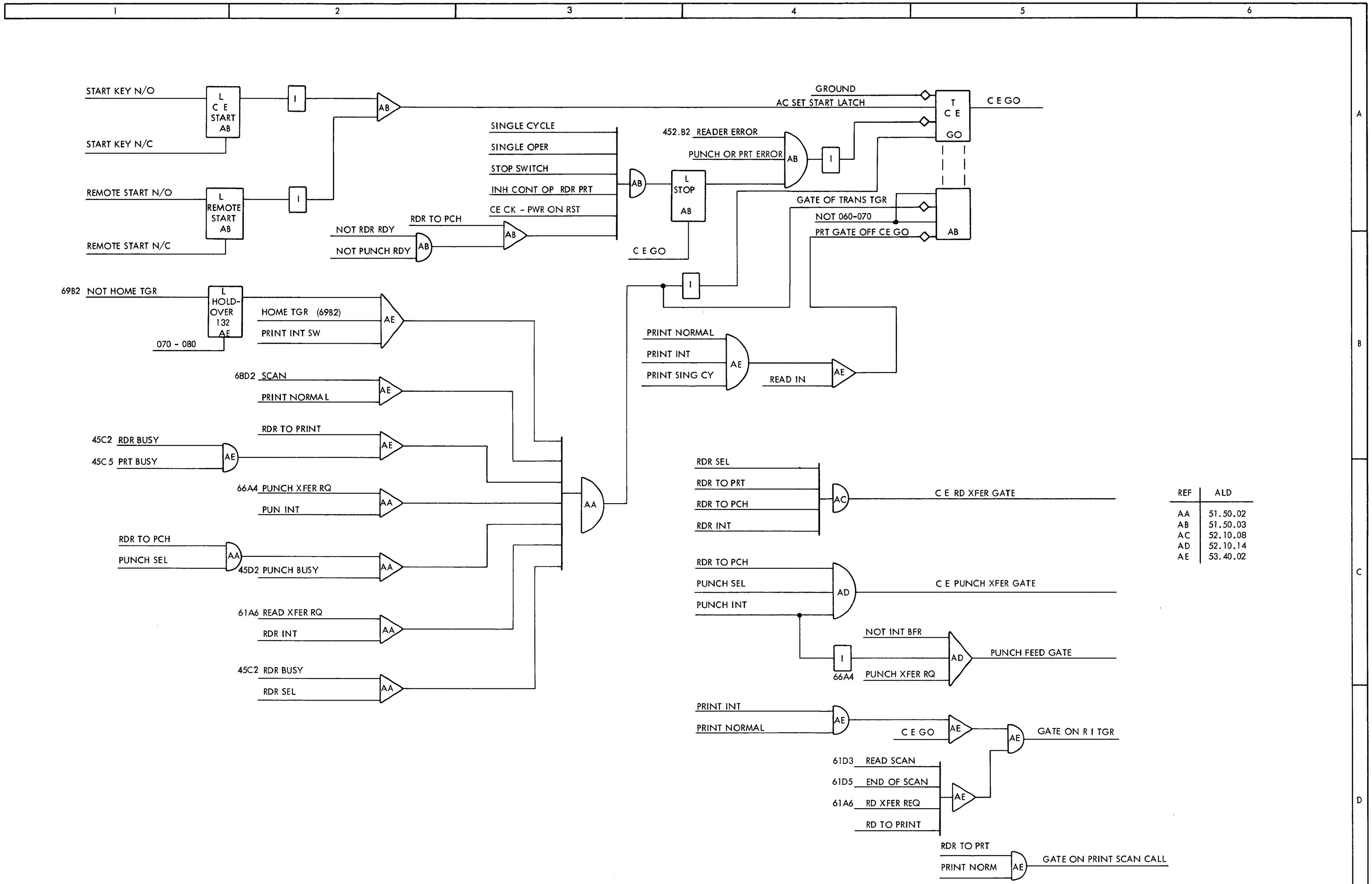


FIGURE 66. PUNCH CONTROL



REF	ALD
AA	51.50.02
AB	51.50.03
AC	52.10.08
AD	52.10.14
AE	53.40.02

FIGURE 67. 1414-3 C E GO

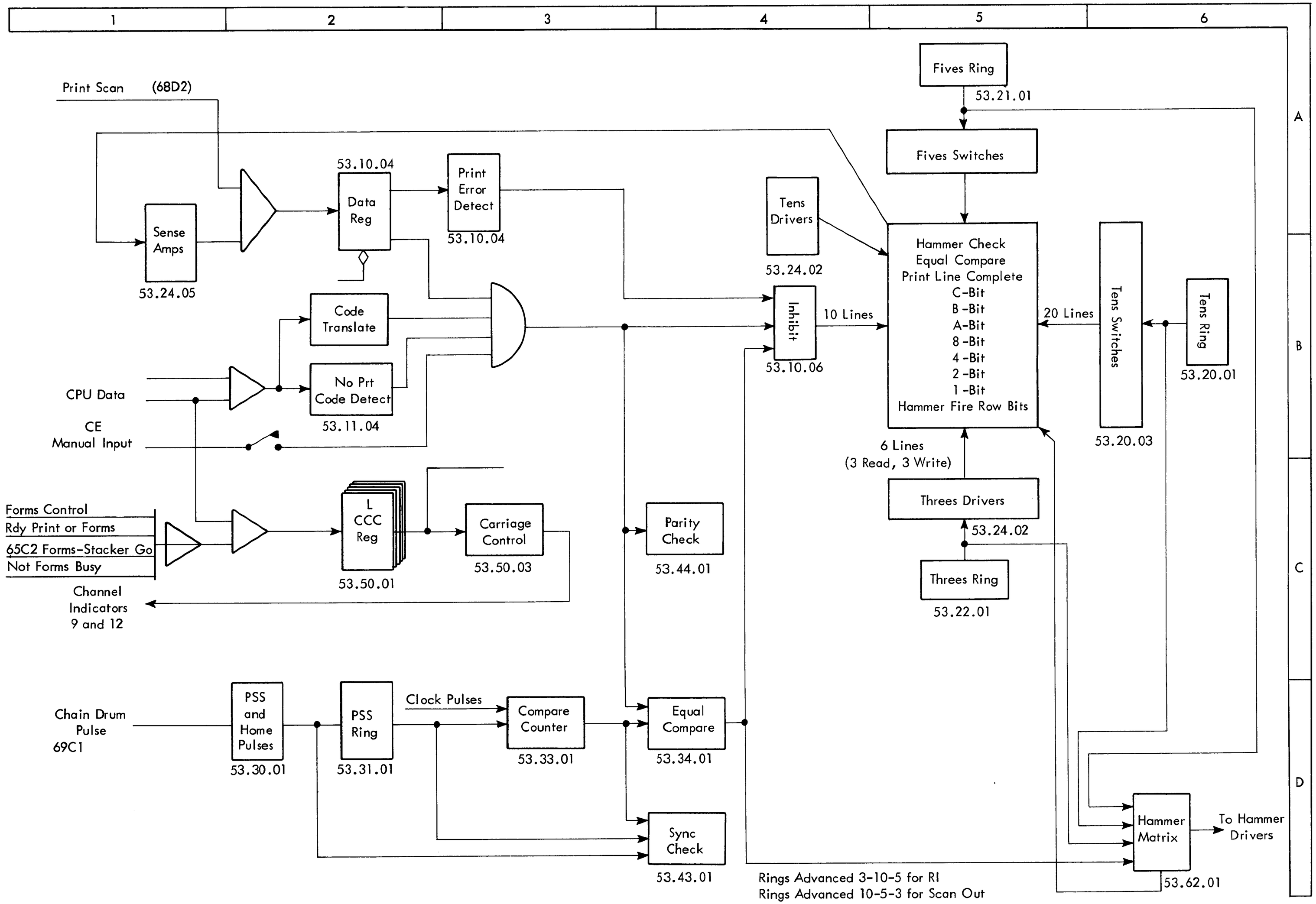


FIGURE 68A. PRINT STORAGE DATA FLOW

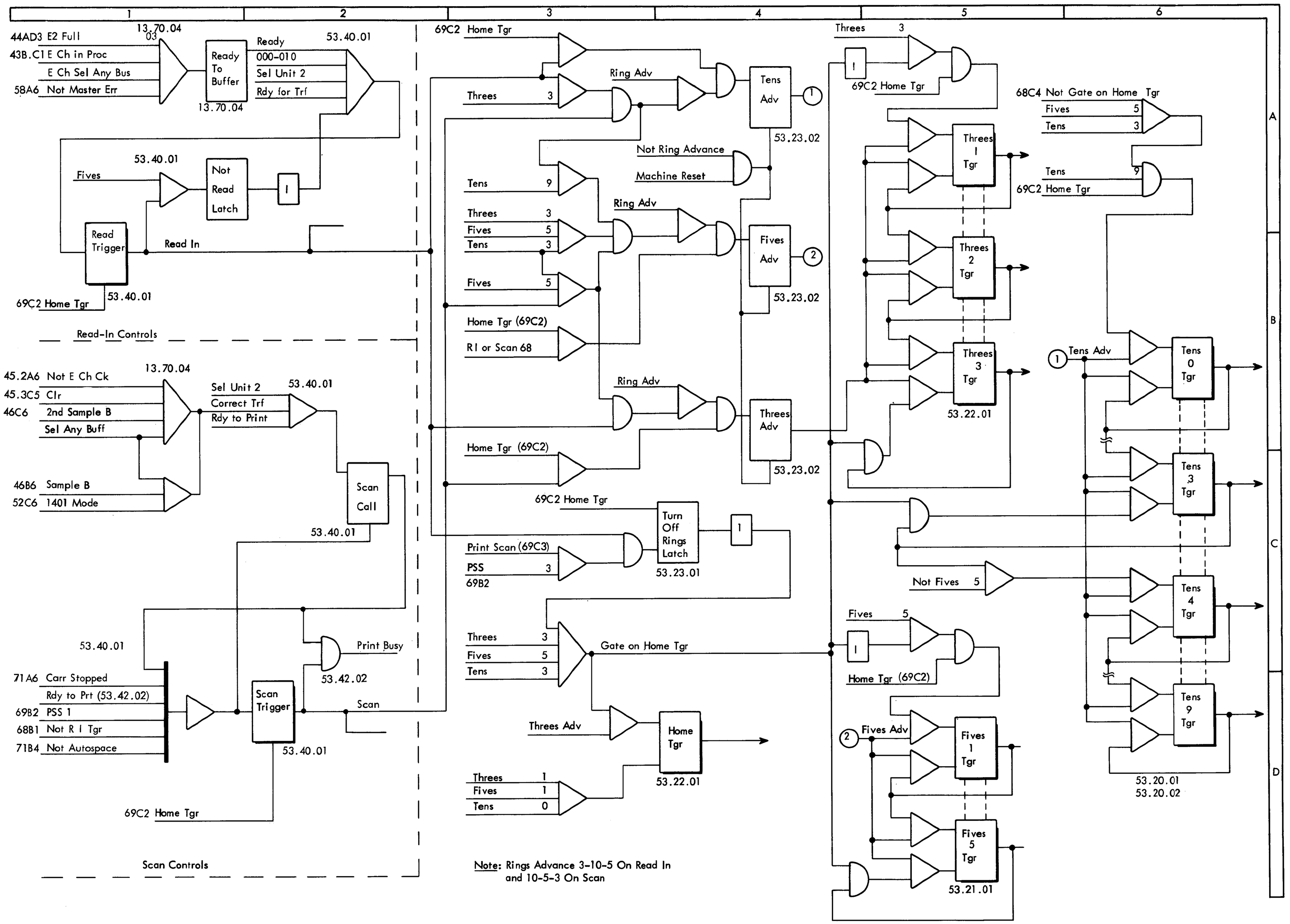


FIGURE 68. PRINT CTRL AND PRINT BFR RINGS

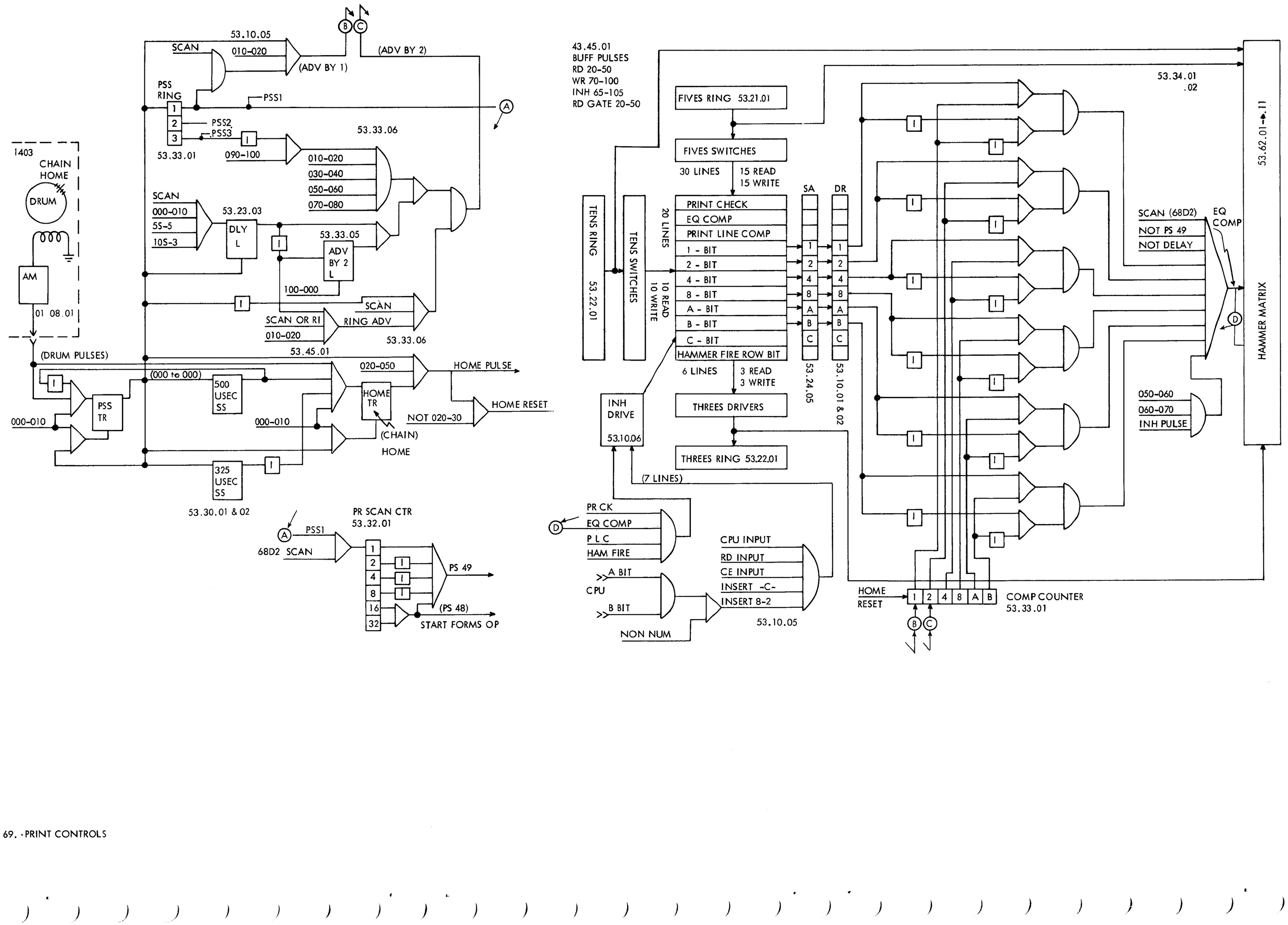


FIGURE 69. · PRINT CONTROLS

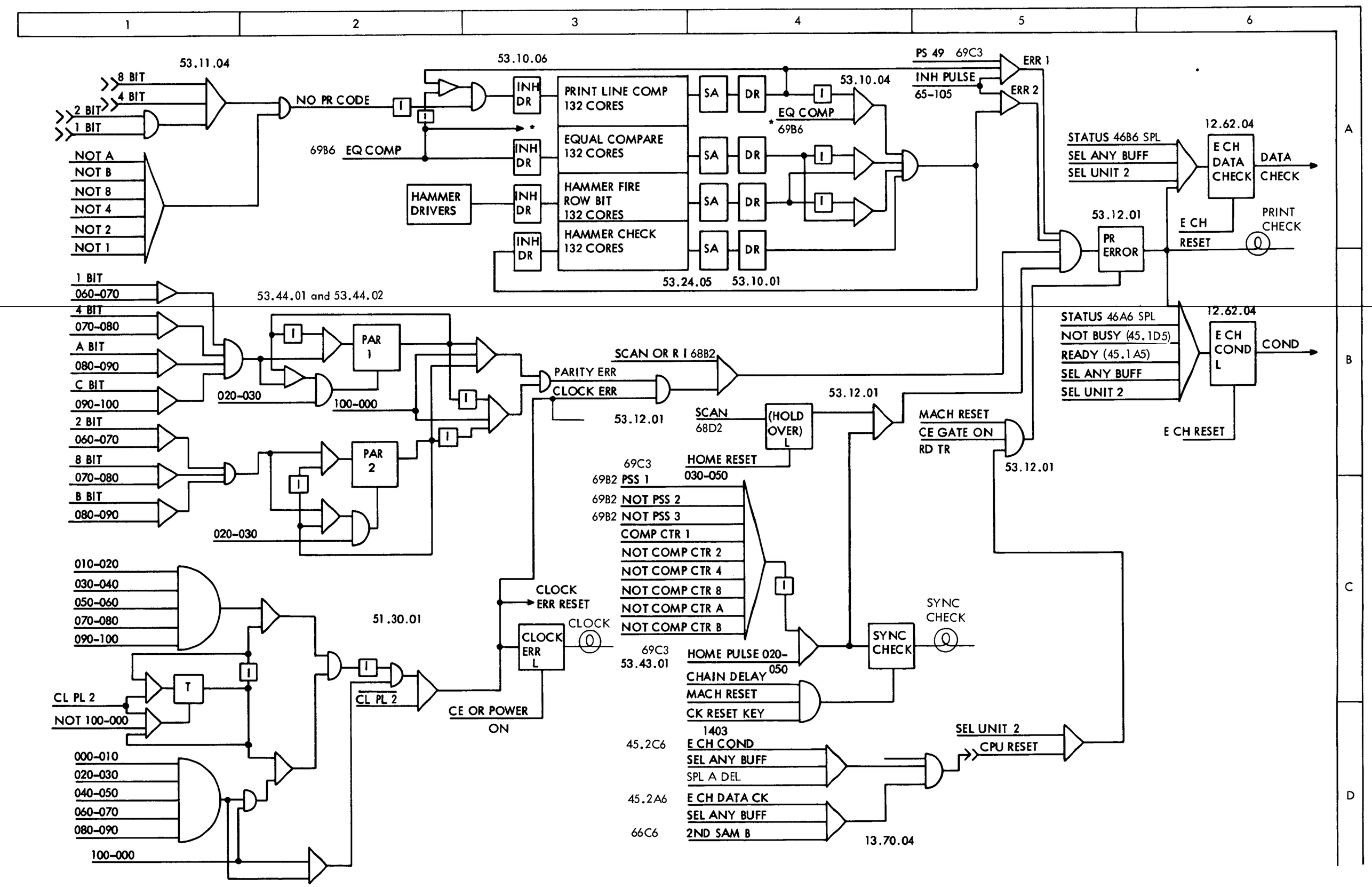


FIGURE 70. PRINT ERROR CIRCUITS

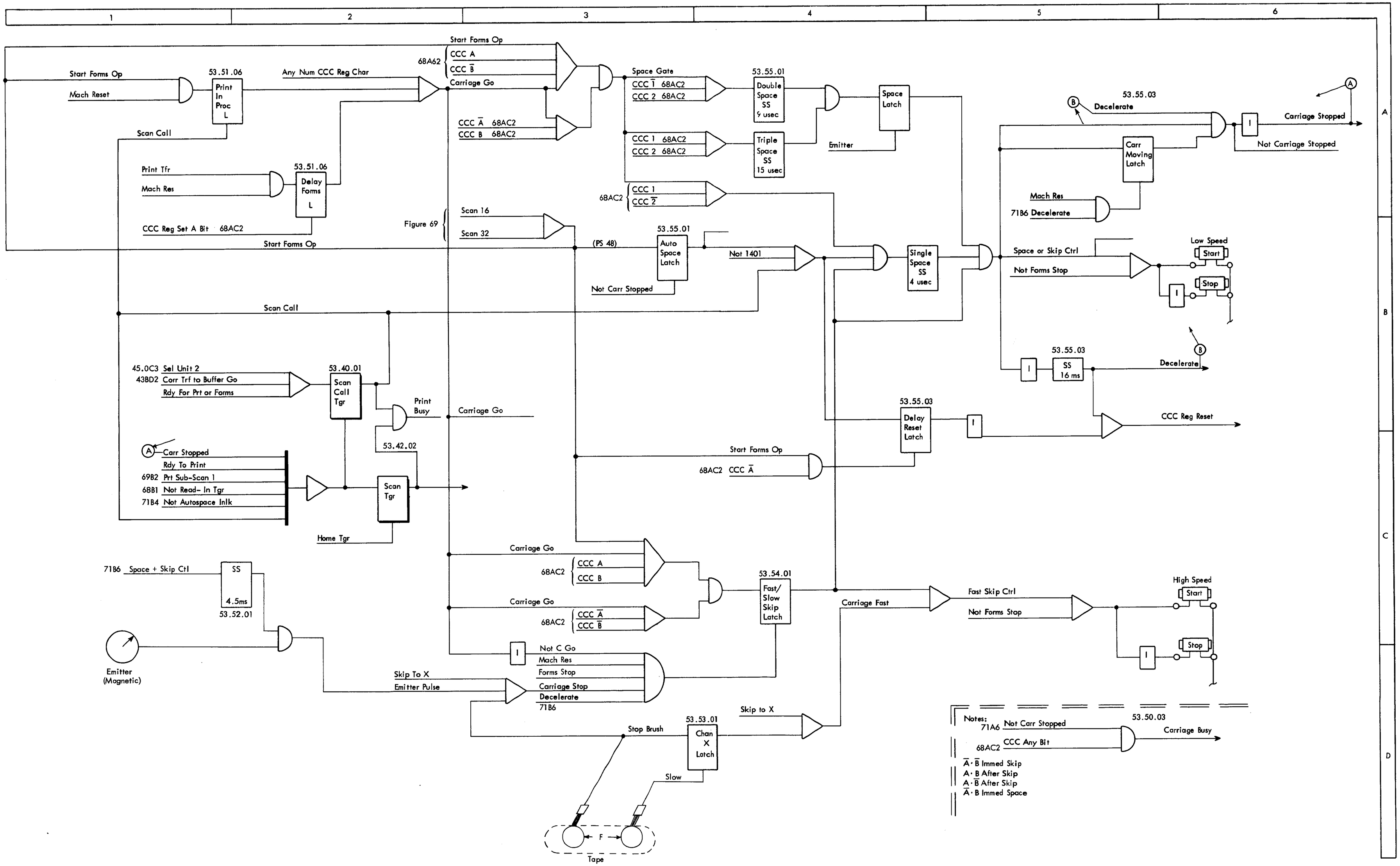


FIGURE 71. CARRIAGE CONTROL

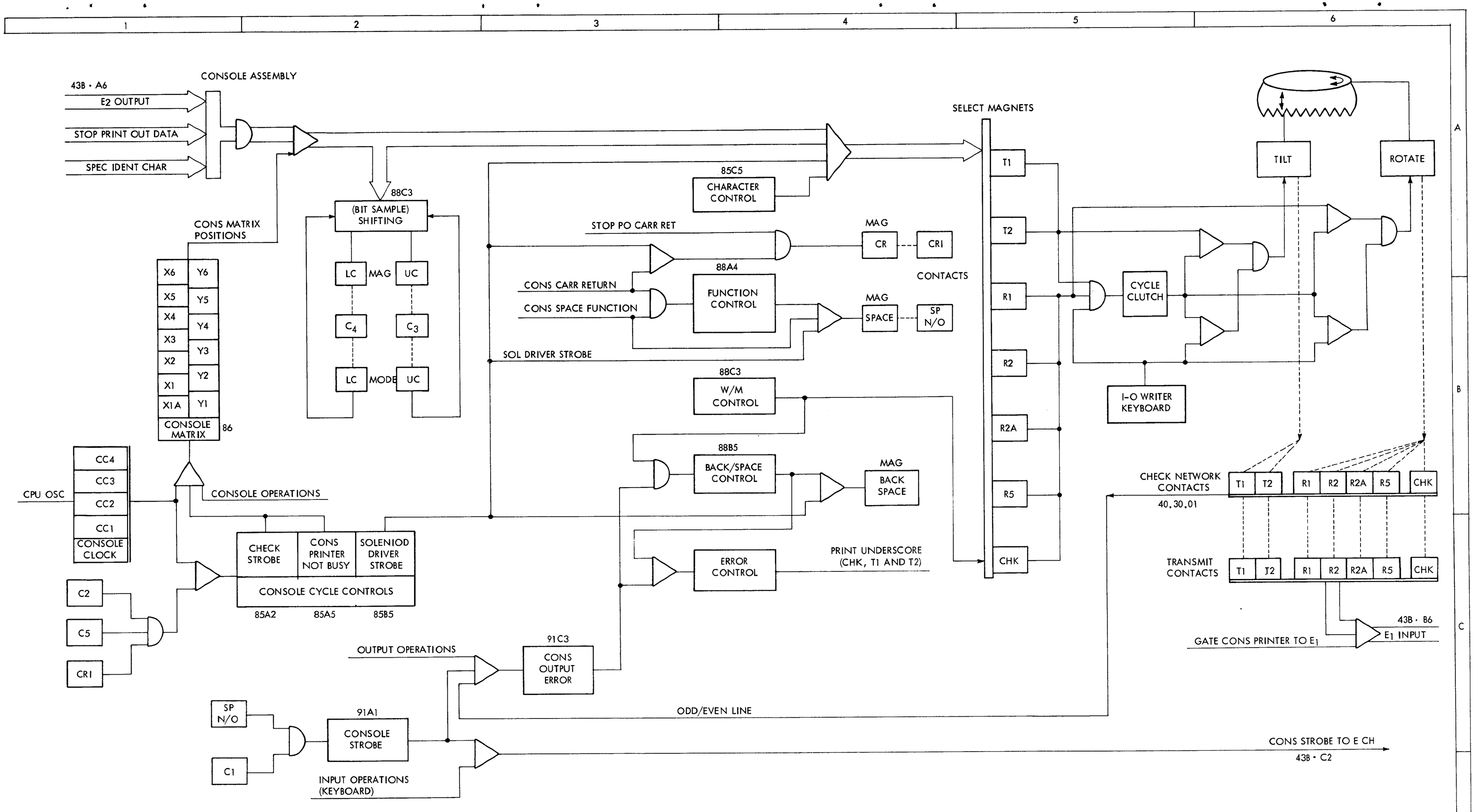


FIGURE 85A. CONSOLE DATA FLOW AND CONTROL

AA - 45.50.01
AB - 45.30.01
AC - 45.50.03
AD - 45.50.08
AE - 45.50.10
AF - 45.50.06
AG - 45.50.07

88D2 NOT KEYBOARD UNLOCK
85B5 CONS CHAR CONTROL
88B5 NOT CONS BACKSPACE CONTROL
91C3 NOT CONSOLE OUTPUT ERROR
88B5 NOT CONS BACKSPACE CONTROL
91C3 CONS ERROR CONTROL
CONS FN CONTROL 88A4
CONS PRINTER NOT BUSY SET

CONS PRINTER C2 N/O
CONS PRINTER C5 N/O
CRI N/O
C2 N/O (35°)
CONS CHECK STROBE
T AA
CC3
85B4 CYCLE LATCH RESET
SS 20 MS
I

CC4
CONS CYCLE LCH SET
NOT CONS PRINTER LAST COL
PROGRAM RESET
88D1 KEYBOARD LOCK SET
CONS CYCLE LATCH RESET
CC1
CONS PRTR NOT BUSY
L AD
CONS PRINTER NOT BUSY
END OF CHAR RESET

CONS PRINTER C2 N/C
CONS PRINTER C5 N/C
CRI N/C
C2 N/C (125°)
CC2
PROGRAM RESET
CC1
TYPE START CTRL
L AA
CC3

88D2 NOT KEYBOARD UNLOCK
85C4 CONS CHAR CONTROL
PRINTER LOCKED CND
CONS PRINTER END OF LINE
88A4 CONSOLE FUNT. CONTROL
88C3 CONS WM CONTROL
91C3 CONS ERROR CONTROL
88B5 CONS BACKSPACE CONTROL

KEYBOARD UNLOCK SET
CC4
CC1
PROGRAM RESET
L TYPE START AC
CONS PRTR SHIFT COMP (88C5)
SOLENOID DRIVER STROBE
L AC
I
8986 NOT CONSOLE OUT 2 BIT
AF
R-1

NOT CONS MX 28 POS
NOT CONS MX 29 POS
88D2 NOT ALTER KEYBOARD UNLOCK
88D2 NOT INQUIRY KEYBOARD UNLOCK
85B5 CONS PRINTER NOT BUSY
88D2 NOT ADDR SET UNLOCK
88B2 PRINTER LOCKED CND PROCEED
NOT DISPLAY WM CTL
90B6 NOT MASTER ERROR
CONS STROBE GATE
NOT CONS MX 32 & 33 POS
NOT CONS HOME POS
AB
TAKE CONS PRINTER CYCLE

CC3
88B5 NOT CONS SPACE FUNCTION
NOT CONS CAR RET
SET FIRST CYCLE LATCH
89B6 NOT CONS OUTPUT WM
88D1 KEYBOARD UNLOCK SET
L CONS CHAR CTL AE
89B6 NOT CONSOLE 8 BIT
NOT CONSOLE 4 BIT
R2A
89B6 NOT CONSOLE 4 BIT
NOT CONSOLE 8 BIT
R2

PROGRAM RESET
88D1 KEYBOARD LOCK SET
88C2 CONS WM INPUT SET
85B4 CONS CYCLE LATCH SET
88C4 NOT CONS WM CONTROL
88B5 CONS BACK SPACE CONTROL
91C3 NOT CONS OUTPUT ERROR
CONS CYCLE LATCH RES 85B4
89B6 NOT CONS 1 BIT
CONS 8 BIT
CONS 1 BIT
NOT CONS 8 BIT
AG
R5

91C3 CONS OUTPUT ERROR
85B5 CONS PRINTER NOT BUSY
CONS PRINTER END OF LINE

NOT CONS 4 BIT
85C5 CONS CHAR CONTROL
91C3 CONS ERROR CONTROL
NOT CONS 8 BIT
88C4 CONS WM CONTROL
89B6 CONS OUT C BIT
CONS OUT CBA 8 2 1 BIT
CONS ERROR CONTROL 91C3
T-1
T-2
CHK

BCD BITS	MAGNETS PICKED
$\overline{2}$	R1
$\overline{8} \cdot \overline{4}$	R2
$\overline{8} + 4$	R2A
$(8 \cdot \overline{1}) + (\overline{8} \cdot 1)$	R5
$\overline{A}$	T1
$\overline{B}$	T2
$C + (C \cdot B \cdot A \cdot 8 \cdot \overline{4} \cdot 2 \cdot 1)$	CHK
$(\overline{8} \cdot 4 \cdot 2 \cdot \overline{1}) + (8 \cdot 4)$	UC (UPPER CASE)
ALL OTHERS	LC (LOWER CASE)
˅(WORD MARK)	UC · CHK
_(UNDERSCORE)	UC · CHK · T1 · T2

OUTPUT TRANSLATOR (+ = OR)
1. WORD MARK - PERIOD (.) CHARACTER (· = AND)

FIGURE 85. CONSOLE CONTROL

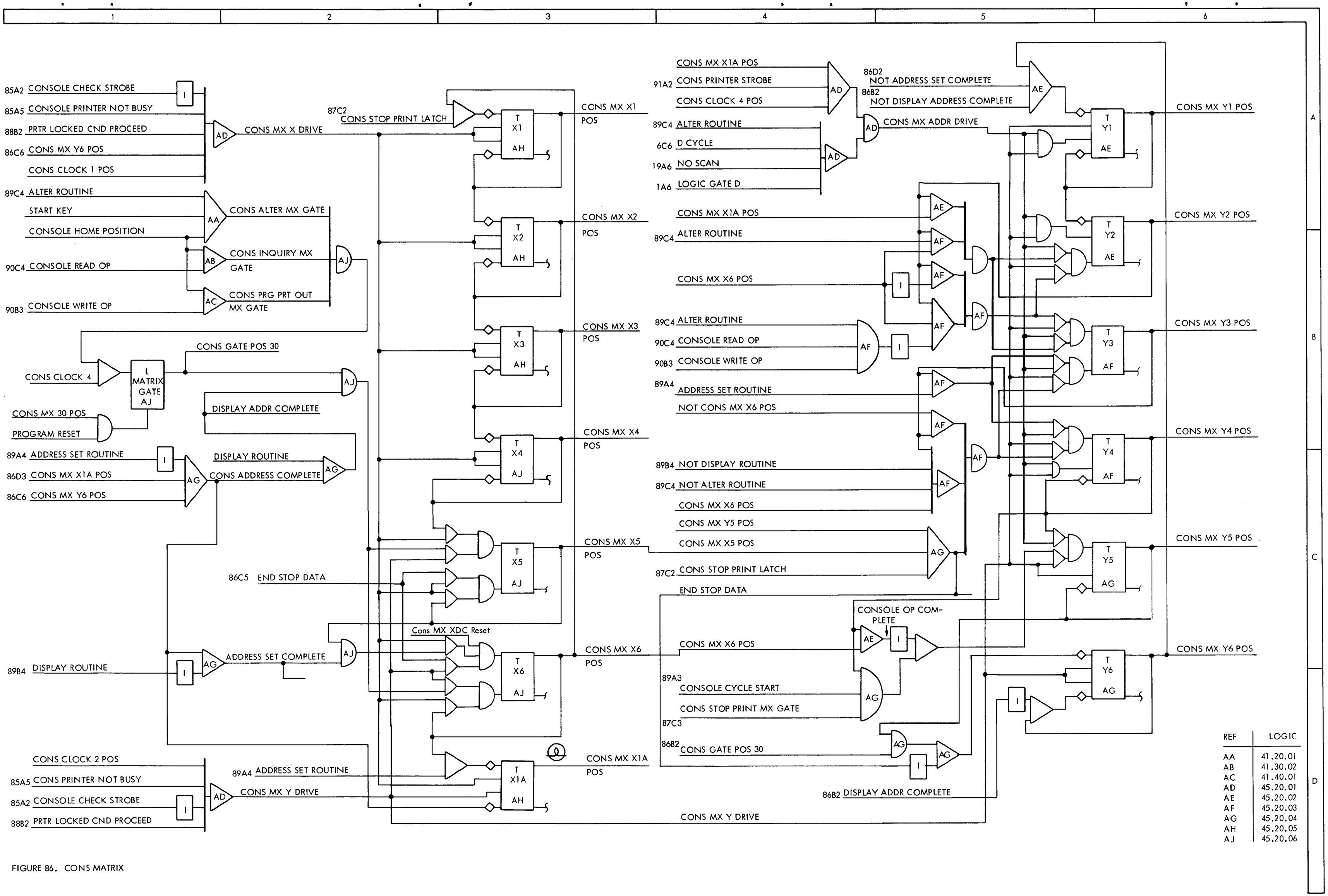


FIGURE 86. CONS MATRIX

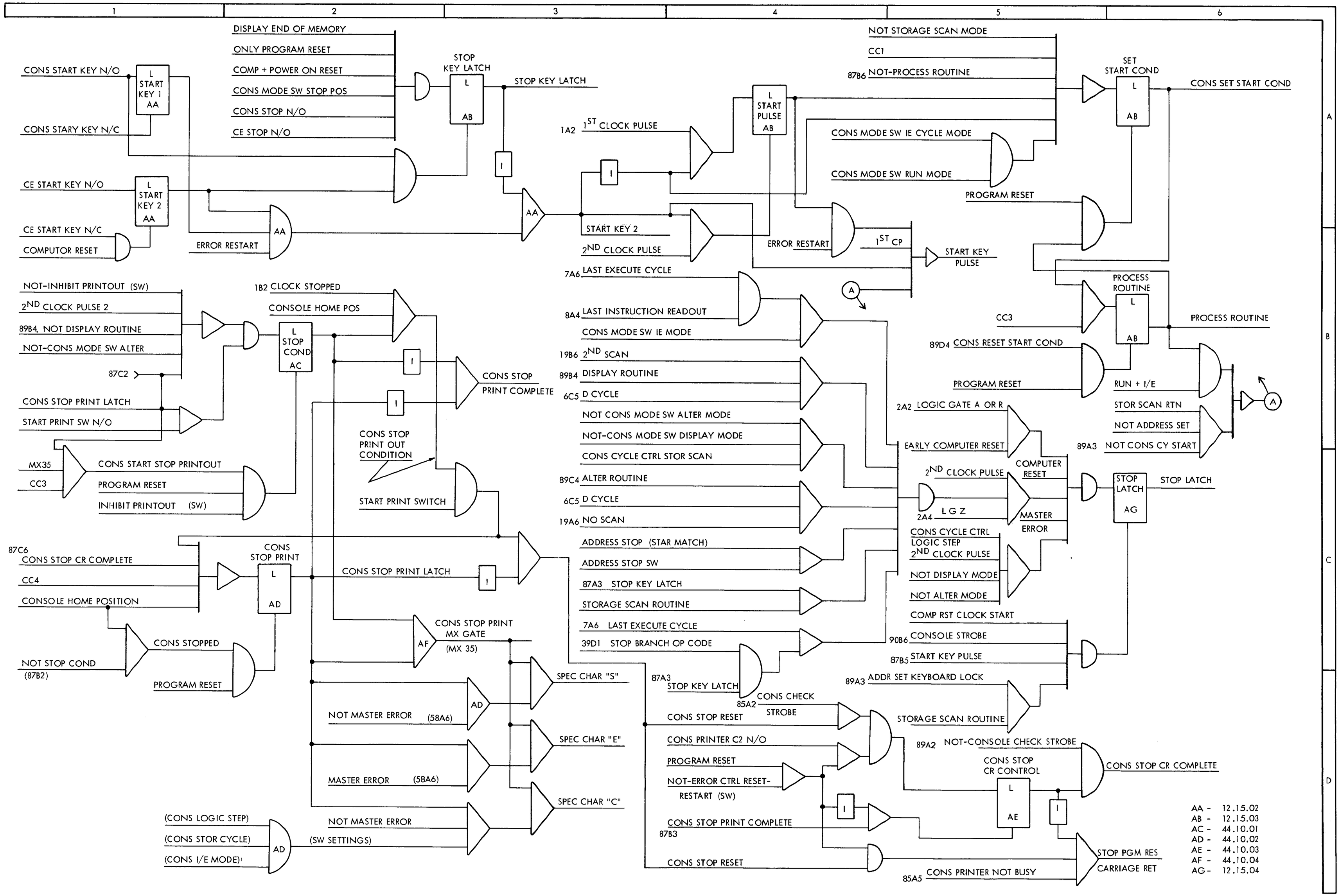


FIGURE 87. CONS START-STOP

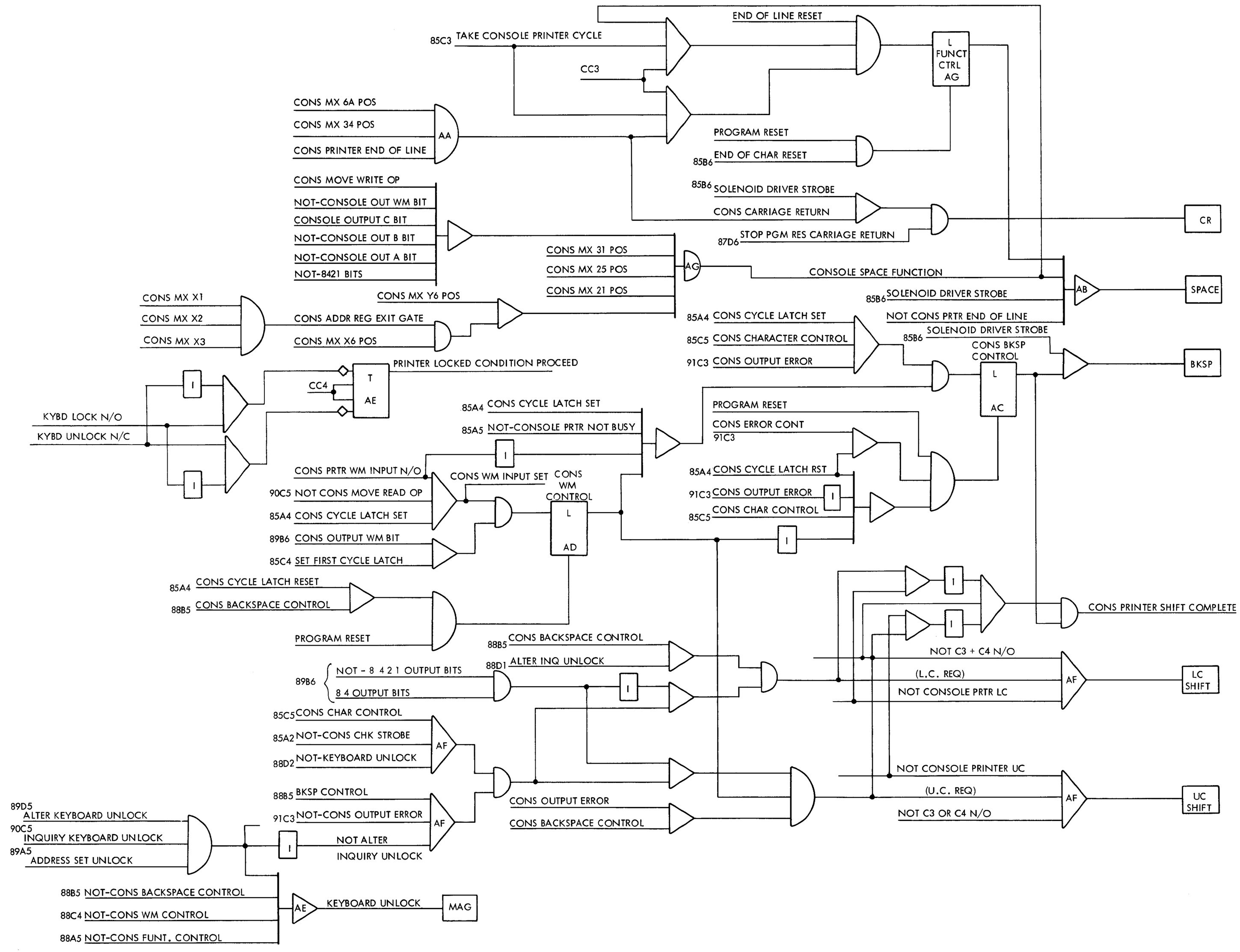
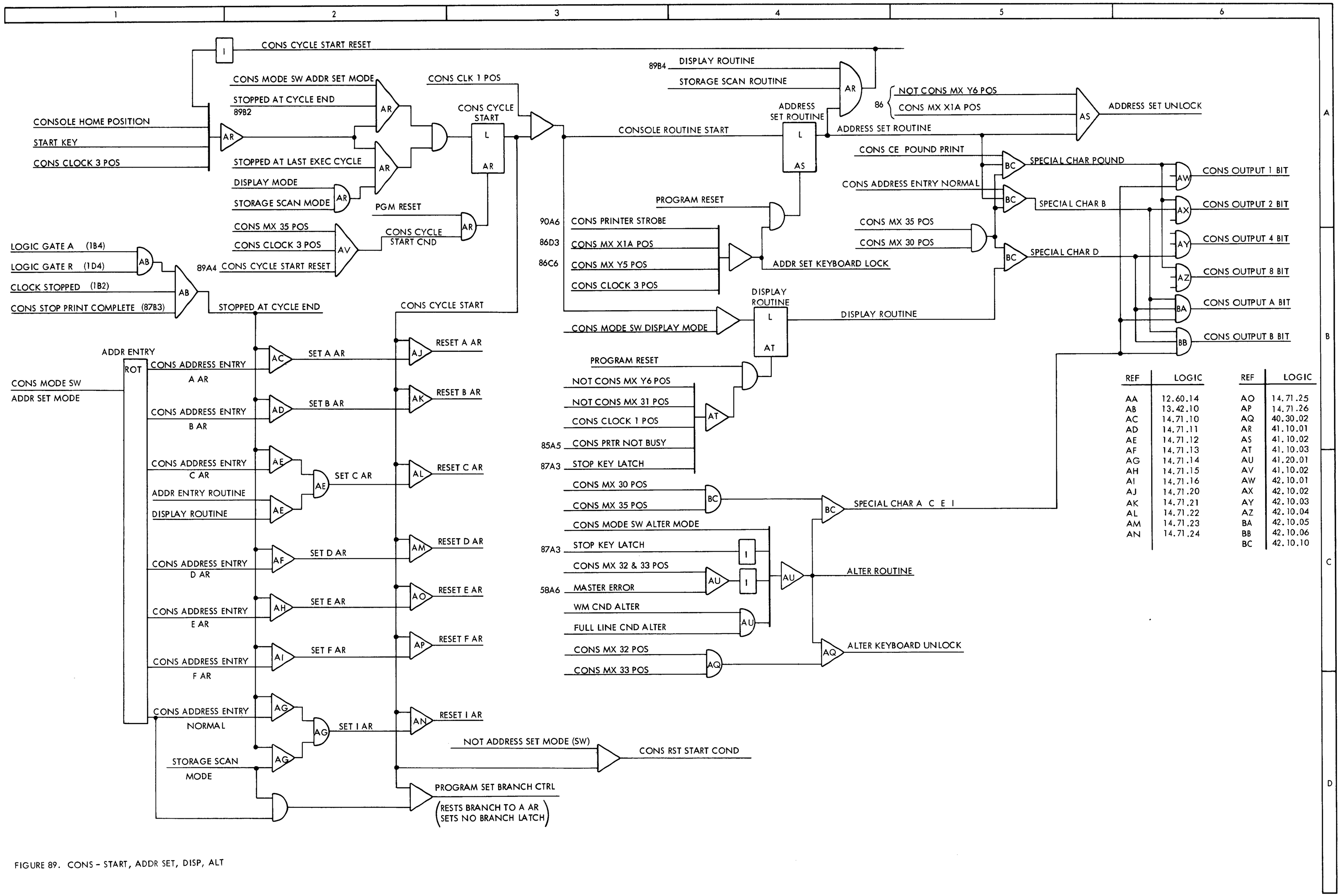


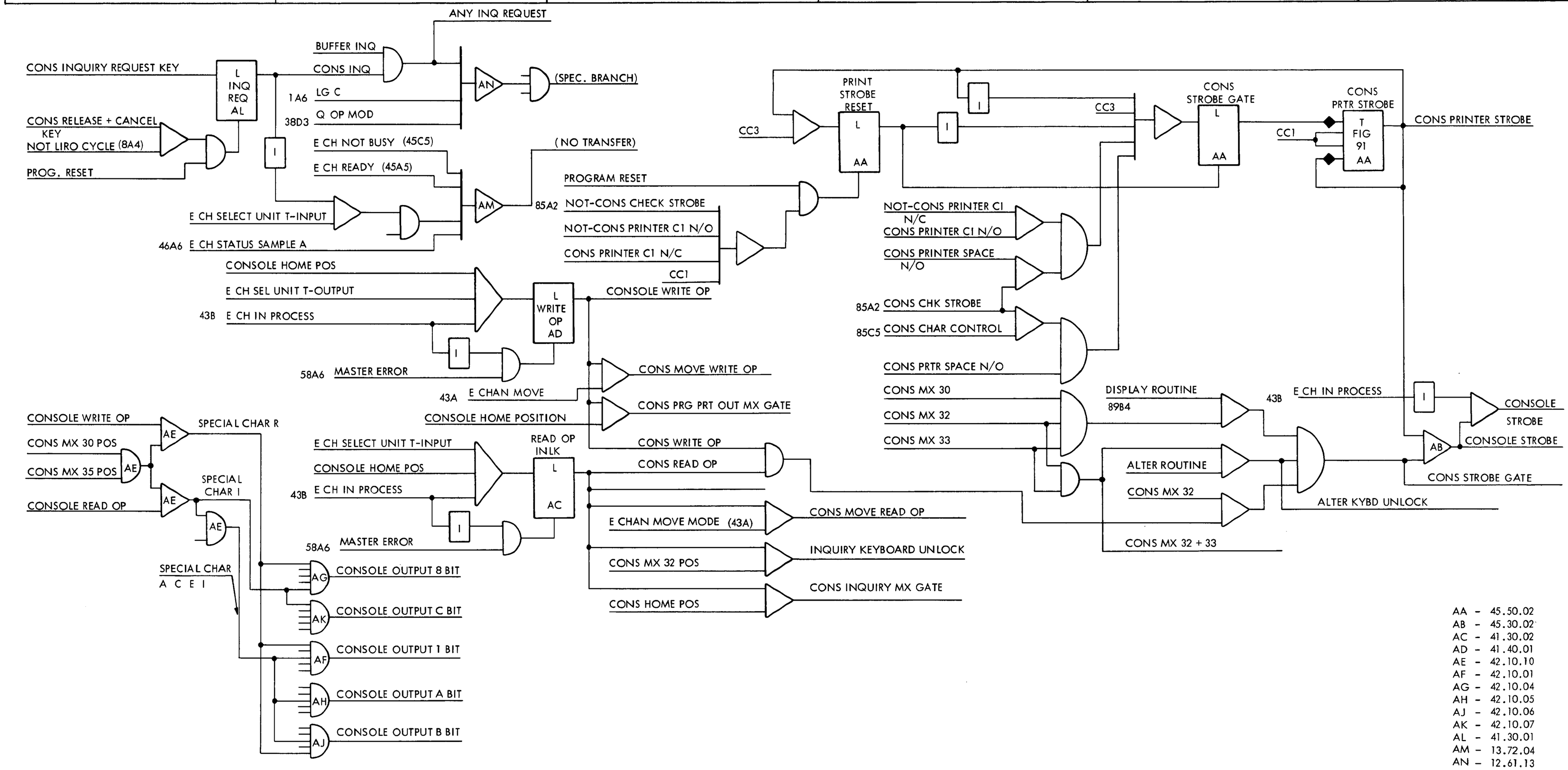
FIGURE 88. CONS FUNCTION CTRL

AA - 45.50.15
AB - 45.50.07
AC - 45.50.13
AD - 45.50.09
AE - 45.50.16
AF - 45.50.05
AG - 45.50.14



REF	LOGIC	REF	LOGIC
AA	12.60.14	AO	14.71.25
AB	13.42.10	AP	14.71.26
AC	14.71.10	AQ	40.30.02
AD	14.71.11	AR	41.10.01
AE	14.71.12	AS	41.10.02
AF	14.71.13	AT	41.10.03
AG	14.71.14	AU	41.20.01
AH	14.71.15	AV	41.10.02
AI	14.71.16	AW	42.10.01
AJ	14.71.20	AX	42.10.02
AK	14.71.21	AY	42.10.03
AL	14.71.22	AZ	42.10.04
AM	14.71.23	BA	42.10.05
AN	14.71.24	BB	42.10.06
		BC	42.10.10

FIGURE 89. CONS - START, ADDR SET, DISP, ALT



AA - 45.50.02
AB - 45.30.02
AC - 41.30.02
AD - 41.40.01
AE - 42.10.10
AF - 42.10.01
AG - 42.10.04
AH - 42.10.05
AJ - 42.10.06
AK - 42.10.07
AL - 41.30.01
AM - 13.72.04
AN - 12.61.13

FIGURE 90. CONS RD-WR OP

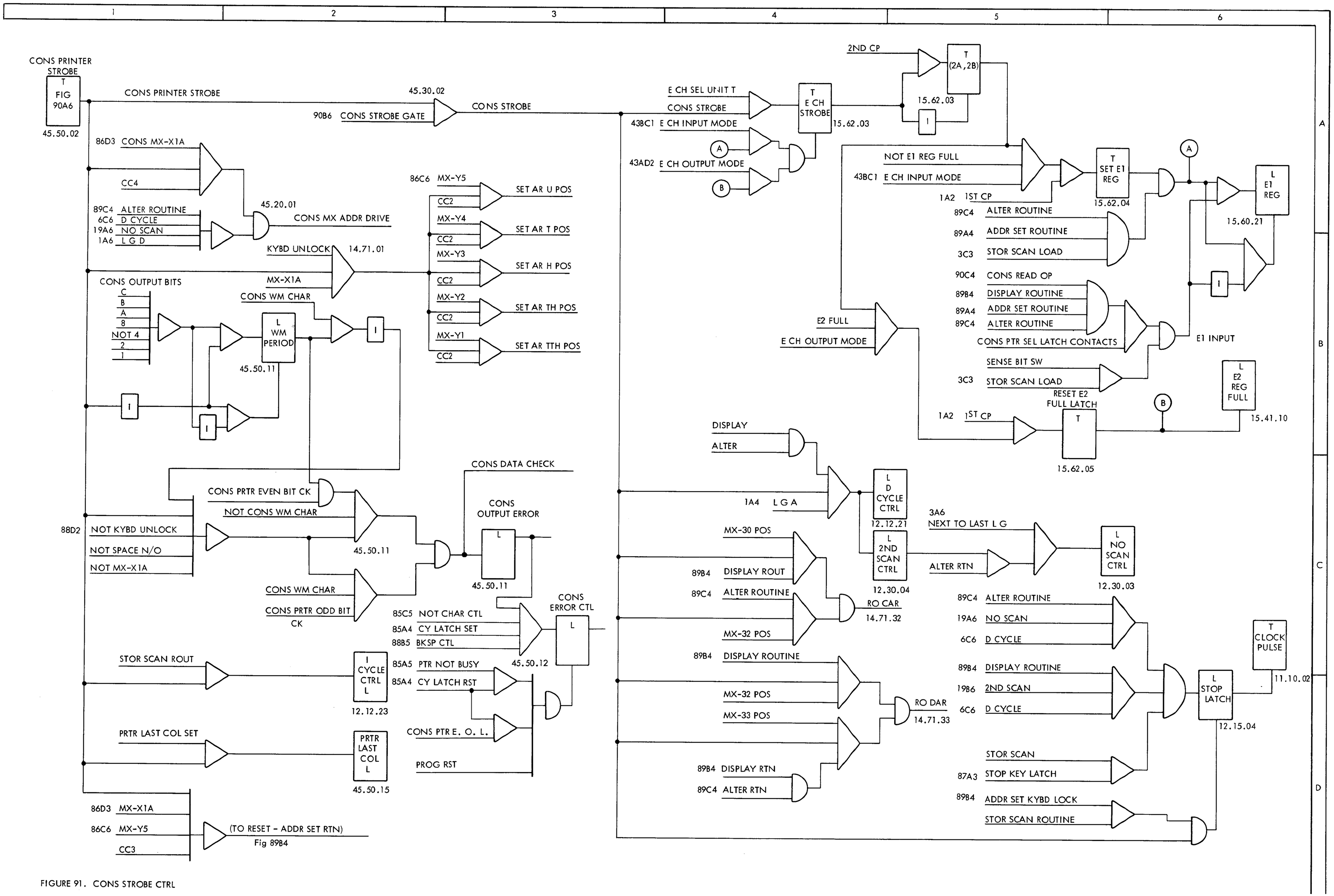


FIGURE 91. CONS STROBE CTRL

INPUTS FROM 729 TAPE DRIVE

02.20.0

729 TP DRV LOGIC		TAPE SYNC ILD
01.03.1	8VPP READ BUS 1 BIT 729	190B1
01.03.1	8VPP READ BUS 2 BIT 729	190B1
01.03.1	8VPP READ BUS 4 BIT 729	190B1
01.03.1	8VPP READ BUS 8 BIT 729	190B1
01.03.1	8VPP READ BUS A BIT 729	190B1
01.03.1	8VPP READ BUS B BIT 729	190B1
01.03.1	8VPP READ BUS C BIT 729	190B1
01.02.1	SEL + RDY WR 729	189A4
01.02.1	SEL + RDY RD 729	189A3
01.09.1	SEL + REWIND 729	185A2
01.05.1	SEL + TI ON 729	183A2
01.02.2	HIGH DENSITY 729	189A1
01.04.1	WRITE ECHO 729	191A1
01.06.1	SEL + LP 729	185A4
01.06.1	SEL + NOT LP 729	189C4
01.05.1	SEL + TI OFF 729	189C4
01.01.1	SEL AND READY MOD 2 729	189A3
01.01.1	SEL AND READY MOD 4 729	189A2
	MOD 5 OR MOD 6	189A2

OUTPUTS TO 729 TAPE DRIVE

02.25.0

TAPE SYNC ILD		729 TP DRV LOGIC
190A4	WRITE BUS 1 BIT 729	01.04.1
190A4	WRITE BUS 2 BIT 729	01.04.1
190A4	WRITE BUS 4 BIT 729	01.04.1
190A4	WRITE BUS 8 BIT 729	01.04.1
190A4	WRITE BUS A BIT 729	01.04.1
190A4	WRITE BUS B BIT 729	
190A4	WRITE BUS C BIT 729	01.04.1
182D2	WRITE PULSE 729	01.04.1
182D6	WR TR REL 729	01.04.1
181C5	SET WR STATUS 729	01.02.1
183C6	SET READ STATUS 729	01.02.1
185C5	BACKWARD 729	01.07.1
189C6	GO 729	01.07.1
185B2	REWIND 729	01.09.1
185D2	REWIND UNLOAD 729	01.09.1
189D3	TURN OFF TI 729	01.05.1
183D2	TURN ON TI 729	01.05.1

INPUTS FROM 7330 TAPE DRIVE

02.21.1

7330 TP DRV LOGIC		TAPE SYNC ILD
73.00.30.0	8VPP READ BUS 1 BIT 7330	190B1
73.00.30.0	8VPP READ BUS 2 BIT 7330	190B1
73.00.30.0	8VPP READ BUS 4 BIT 7330	190B1
73.00.30.0	8VPP READ BUS 8 BIT 7330	190B1
73.00.30.0	8VPP READ BUS A BIT 7330	190B1
73.00.30.0	8VPP READ BUS B BIT 7330	190B1
73.00.30.0	8VPP READ BUS C BIT 7330	190B1
73.00.30.0	SEL + RDY WR 7330	189A4
73.00.30.0	SEL + RDY RD 7330	189A3
73.00.30.0	SEL + REWIND 7330	185A1
73.00.30.0	SEL + TI ON 7330	183A1
73.00.30.0	SEL + RDY HI 7330	189A2
73.00.30.0	ECHO PULSE 7330	191A1
73.00.30.0	SEL + LP 7330	185A4
73.00.30.0	SEL + RDY LO 7330	189A2
73.00.30.0	SEL RDY BWKD 7330	185C3

OUTPUTS TO 7330 TAPE DRIVE

02.26.0

TAPE SYNC ILD		7330 TP DRV LOGIC
190B1	WRITE BUS 1 BIT 7330	73.00.20.0
190B1	WRITE BUS 2 BIT 7330	73.00.20.0
190B1	WRITE BUS 4 BIT 7330	73.00.20.0
190B1	WRITE BUS 8 BIT 7330	73.00.20.0
190B1	WRITE BUS A BIT 7330	73.00.20.0
190B1	WRITE BUS B BIT 7330	73.00.20.0
190B1	WRITE BUS C PIT 7330	73.00.20.0
182D2	WRITE PULSE 7330	73.00.20.0
182D5	WR TR REL 7330	73.00.20.0
181C5	SET WRITE STATUS 7330	73.00.20.0
183C6	SET READ STATUS 7330	73.00.20.0
185C5	BACKWARD 7330	73.00.20.0
189C6	GO 7330	73.00.20.0
185B2	REWIND 7330	73.00.20.0
185D2	REWIND UNLOAD 7330	73.00.20.0
189D3	TURN OFF TI 7330	73.00.20.0
183D2	TURN ON TI 7330	73.00.20.0

INPUTS TO TAPF SYNC

02.30.0

	TAPE SYNC IID
1 BIT WRITE DATA LINE	190A4
2 BIT WRITE DATA LINE	190A4
4 BIT WRITE DATA LINE	190A4
8 BIT WRITE DATA LINE	190A4
A BIT WRITE DATA LINE	190A4
B BIT WRITE DATA LINE	190A4
C BIT WRITE DATA LINE	190A4
WR CALL	181A5
WR TM CALL	181A6
DISC CALL	182A5
READ CALL	183A6
REWIND CALL	185A2
REWIND + UNLOAD CALL	185B2
BACKSPACE CALL	185A6
ERASE CALL	185A5
TAU RESET	186A1
ODD REDUNDANCY CALL	183A3
TURN OFF TI	189C3
MAN WR DISC	182A5
MANUAL STOP ON ERROR	192B5
MANUAL STOP ON ERROR	192C2
EARLY SAMPLE	192A3
EARLY SAMPLE	191C4
AMPLIFIER BIAS	190A1
COMPARE CHECK CE	192B5
REG A ONLY	191B6
REG B ONLY	191B6
NOT MANUAL OP	181A5
MANUAL ERROR RESET	192A2

OUTPUTS TO CONTROL UNIT

02.35.0

TAPE SYNC ILD	
190A6	R-W REG 1 BIT
190A6	R-W REG 2 BIT
190A6	R-W REG 4 BIT
190A6	R-W REG 8 BIT
190A6	R-W REG A BIT
190A6	R-W REG B BIT
190A6	R-W REG C BIT
181B5	WRITE
182C6	WRITE COND
181D5	BUSY
185B4	LOAD POINT
1880 2	CHECK CHAR
183B1	SEL + TI ON
192C2	ERROR
19202	STOP ON ERROR
182D3	WC 2
182C2	WC 8 TR
184B4	WR RC-5 OR READ RC-7
182C2	WC-4
184D5	RC-3
181C3	WD 320 OR WD 1088
188C6	RDD
181C4	WD 49
185B2	SEL + REWIND
189D4	SEL + NOT LP
189D4	SEL + TI OFF
189C2	SEL + READY MOD 4
189B2	SEL + RDY HI 7330
188B5	RDD-36
188B4	RDD 144
188B1	COMPUTE
185C5	BACKWARD

FIGURE 180. TAU INDEX

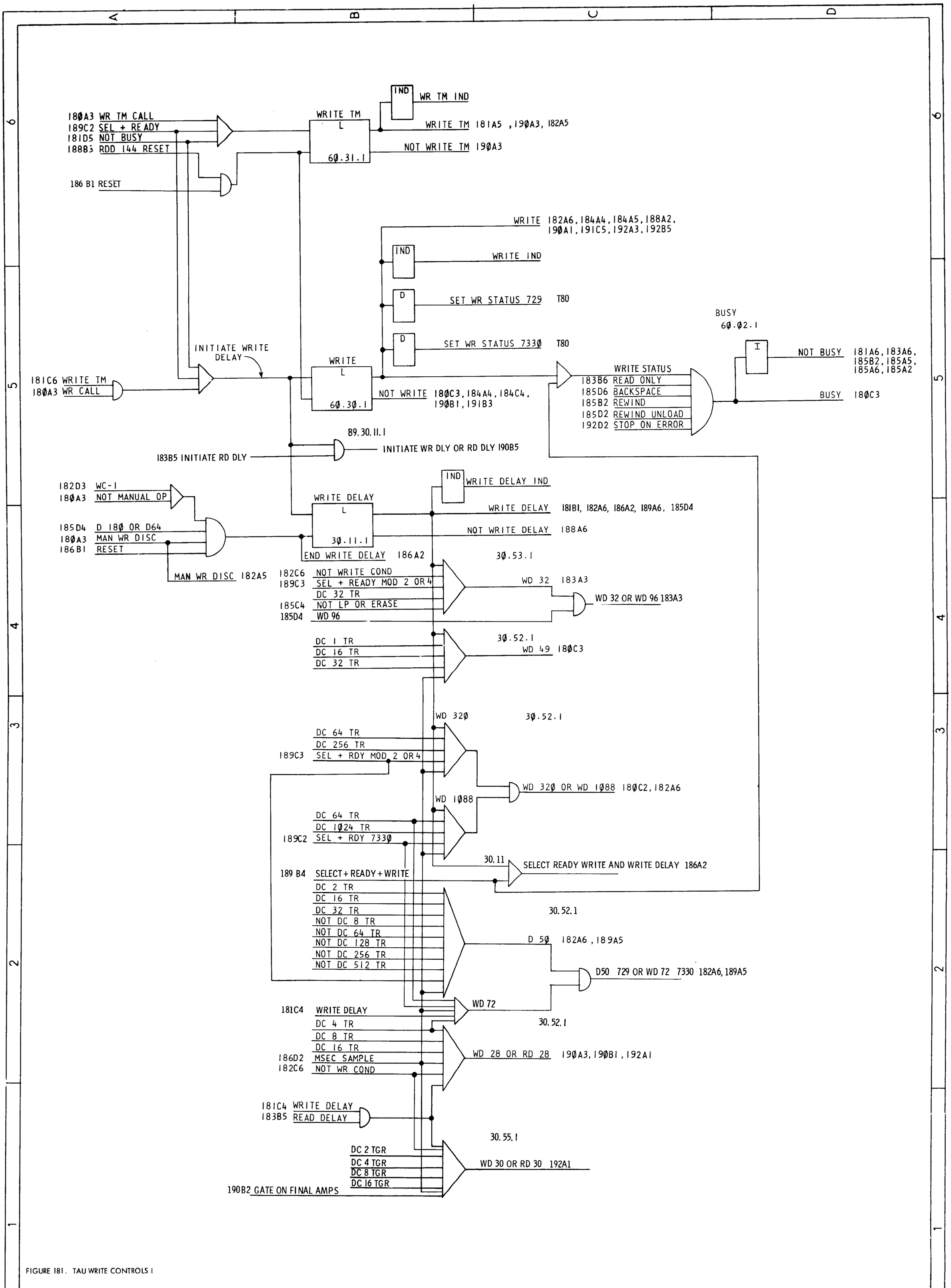


FIGURE 181. TAU WRITE CONTROLS I

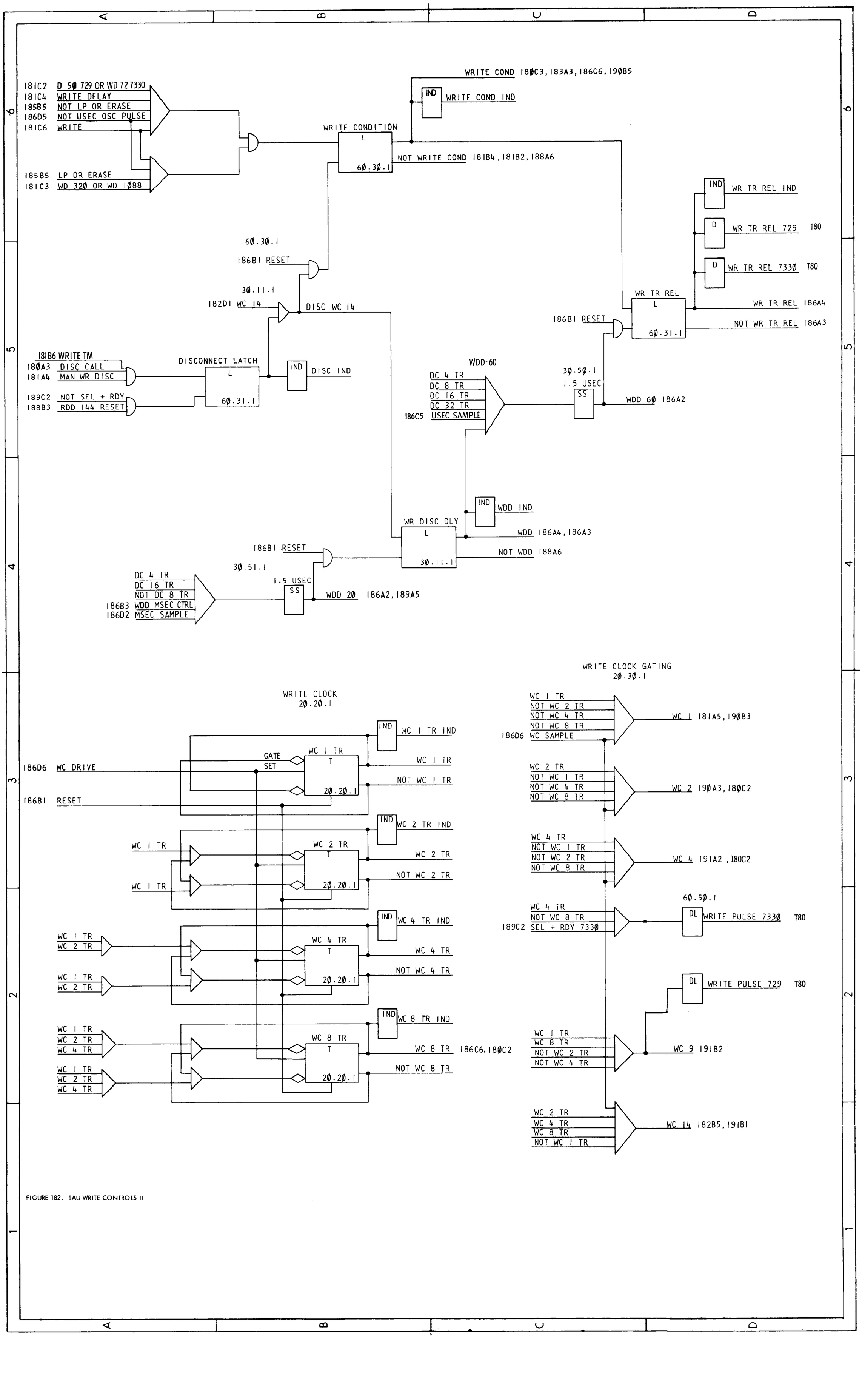


FIGURE 182. TAU WRITE CONTROLS II

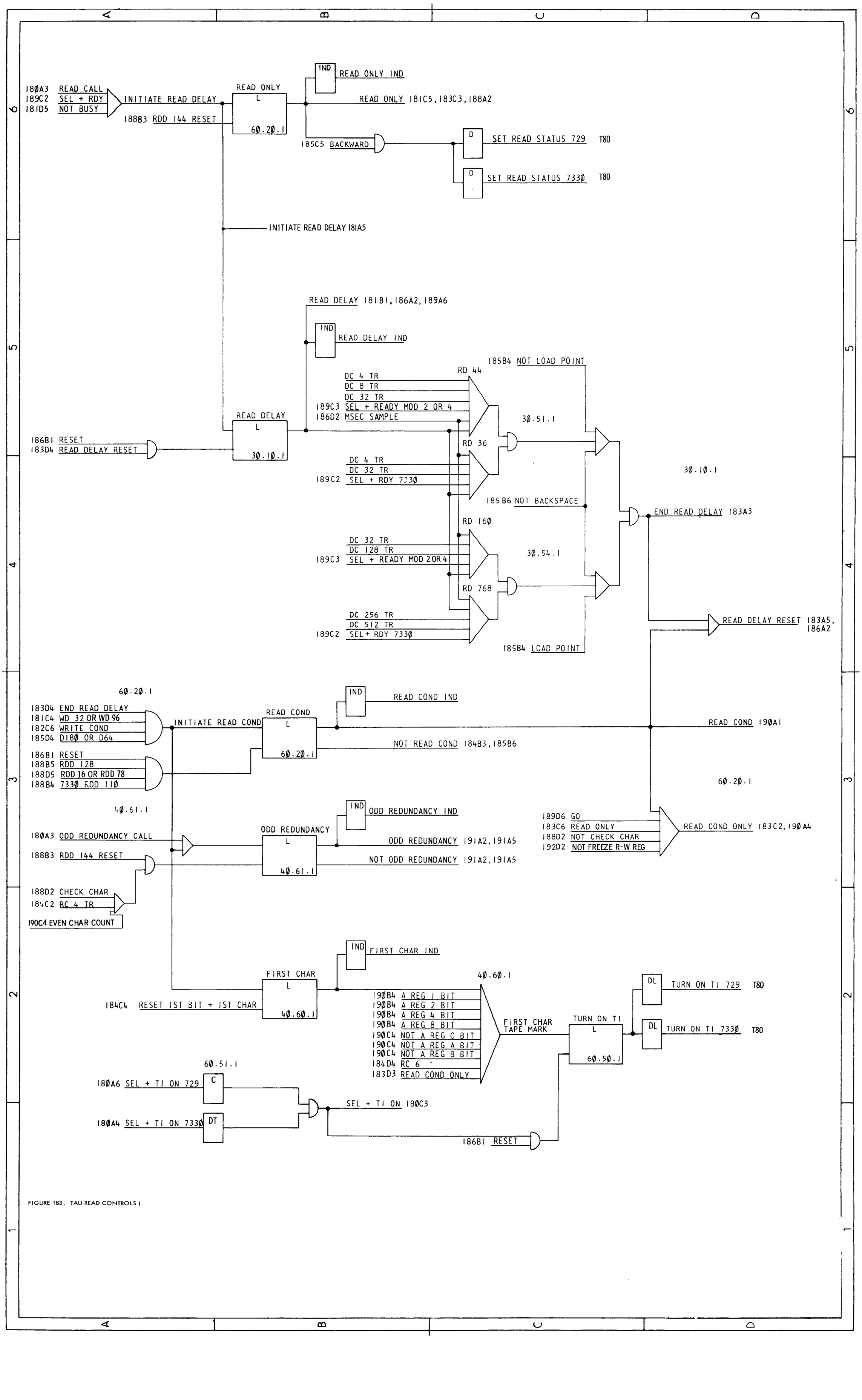


FIGURE 183. TAU READ CONTROLS 1

READ RECOGNITION
40.60.1

HI CLIP OUTPUT

190C3
HI CHAN 1 BIT
HI CHAN 2 BIT
HI CHAN 4 BIT
HI CHAN 8 BIT
HI CHAN A BIT
HI CHAN B BIT
HI CHAN C BIT

HI CLIP PULSE 192B4

LO CLIP OUTPUT

190B3
LO CHAN 1 BIT
LO CHAN 2 BIT
LO CHAN 4 BIT
LO CHAN 8 BIT
LO CHAN A BIT
LO CHAN B BIT
LO CHAN C BIT

181C6 WRITE

FIRST BIT
L
40.60.1

READ CLOCK OSCILLATOR GATING
10.10.1

IND FIRST BIT IND

1 MC OSC
GATE IN 1MC RD. OSC

360 KC OSC
189C2 SEL + RDY MOD 4
189D1 NOT HIGH DENSITY 729

667 KC OSC
GATE IN 667 KC
RD OSC

240 KC OSC
DENSITY 200 SEL
RDY MOD 2 OR 5

320 KC OSC
189D1 SEL + RDY HI 7330

115 KC OSC
189C2 SEL + RDY LO 7330

FIRST BIT 190D3

I
READ CLOCK RESET 184B2

READ CLOCK SAMPLE 184A4

I
READ CLOCK DRIVE 184B3

READ CLOCK GATING
10.30.1

RC 1 TR
RC 2 TR
NOT RC 4 TR
NOT RC 8 TR
RC 3 191B2, 180C2

RC 4 TR
NOT RC 1 TR
NOT RC 2 TR
NOT RC 8 TR
RC 4 188A6, 192A3

RC 2 TR
RC 4 TR
NOT RC 1 TR
181B5 NOT WRITE
RC 6 183B2, 190B3, 192A3

180C6 BACKWARD AT LOAD POINT
I

READ CLOCK GATING
10.31.1

181C6 WRITE
RC 2 TR
181C4 NOT WRITE
NOT RC 2 TR
RC 1 TR
RC 4 TR
WR RC-5 OR READ RC-7 188A6, 190C4, 191B5, 192B5, 192B4

READ ONLY

RC 2 TR
RC 8 TR
NOT RC 1 TR
184D5 READ CLOCK SAMPLE
WRITE

WR RC 10 OR READ RC 7 192B5

Ø.4 USEC
I
SS

186B1 RESET
RESET 1ST BIT + 1ST CHAR. 183A2, 192B3

192D2 NOT STOP ON ERROR
183C3 NOT READ COND
WR RC-10 OR READ RC-7 RESET 190C3

186B1 RESET

READ CLOCK
10.20.1

184D5 READ CLOCK DRIVE
184C5 READ CLOCK RESET

RC 1 TR
T
10.20.1

IND RC 1 TR IND
RC 1 TR
NOT RC 1 TR

RC 1 TR
RC 1 TR

RC 2 TR
T
10.20.1

IND RC 2 TR IND
RC 2 TR
NOT RC 2 TR

RC 1 TR
RC 2 TR
RC 1 TR
RC 2 TR

RC 4 TR
T
10.20.1

IND RC 4 TR IND
RC 4 TR 183A3
NOT RC 4 TR

RC 1 TR
RC 2 TR
RC 4 TR
RC 1 TR
RC 2 TR
RC 4 TR

RC 8 TR
T
10.20.1

IND RC 8 TR IND
RC 8 TR
NOT RC 8 TR

FIGURE 184. TAU READ CONTROLS II

FIGURE 185. TAU UNIT CONTROL

WRITE CLOCK AND DELAY COUNTER OSCILLATOR GATING
20.10.1

960 KC OSC
DENSITY 800 SEL RDY M5

1 MC OSC
189B1 HIGH DENSITY
189C2 SEL + READY MOD 4

360 KC OSC
189B1 NOT HIGH DENSITY
189C2 SEL + READY MOD 4

667 KC OSC
189B2 HIGH DENSITY 729
DENSITY 556
SEL RDY M2+M5

240 KC OSC
DENSITY 200 SEL RDY M2+M5

320 KC OSC
189C2 SEL + RDY HI 7330

115 KC OSC
189C2 SEL + RDY LO 7330

182D5 WR TR REL
182C4 WDD
185B6 NOT BACKSPACE
188C6 RDD
→ USEC CTRL

182C6 WRITE COND
182B2 WC 8 TR
→ WC DRIVE 182B3
I → WC SAMPLE 182C3

I → NOT USEC OSC PULSE 182A6
USEC OSC PULSE

30.20.1
→ USEC SAMPLE 188A5, 182C5

30.20.1
10 KC OSC
189C2 SEL + READY MOD 4
189C2 SEL + RDY 7330
6.7 KC OSC
189C3 SEL + READY MOD 2

30.20.1
→ DC DRIVE 187B6

182C4 WDD
182D5 NOT WR TR REL
→ WDD MSEC CTRL 182A4

188C6 RDD
185D6 BACKSPACE
188B3 FWD STOP DELAY
183B5 READ DELAY
185B6 BKSP NOT READ COND
181C2 SELECT READY WRITE AND WRITE DELAY
→ MSEC SAMPLE 181B2, 182A4, 182C5, 183B5, 185C5, 188C5, 188A2

NOT DC RESET

I → DC RESET 187B6

30.31.1
182B4 WDD 20
182C5 WDD 60
183D4 READ DELAY RESET
188B6 END RDD
181B4 END WRITE DELAY
185D5 7330 WR FWD D 128 THEN BKSP
185C6 BACKWARD AT LOAD POINT
→ 1.5 USEC SS

180A3 TAU RESET → RESET 181, 182, 183, 184, 185, 188, 189, 190, 192

FIGURE 186. TAU WR CLOCK AND DLY CTR OSC GATING

DELAY COUNTER
30.40.1

FIGURE 187. TAU DELAY COUNTER

READ DISCONNECT DELAY
30.10.1

184B4 WR RC 5 OR READ RC-7
181C4 NOT WRITE DELAY
182C6 NOT WRITE COND
182C4 NOT WDD

READ DISC DLY
L
30.10.1

IND
RDD IND

RDD 186A2, 186A4, 191B2, 180C2

NOT RDD 185C4, 185B5, 185B6

188B4 7330 RDD 110
188B3 RDD 144 RESET

END RDD 186A2

184D5 RC 4
188D2 NOT CHECK CHAR

RDD

RDD 16

DC 16 TR
186D2 MSEC SAMPLE
185D6 BACKSPACE
189C3 SEL + READY MOD 2 OR 4

30.50.1

RDD 78

RDD 16 OR 78 183A3

30.51.1

DC 64 TR
DC 4 TR
DC 2 TR
DC 8 TR
189C2 SEL + RDY 7330
185D6 BACKSPACE

RDD 36

DC 4 TR
DC 32 TR
NOT DC 1 TR
NOT DC 2 TR
NOT DC 8 TR
NOT DC 16 TR
NOT DC 64 TR
NOT DC 128 TR
186C5 USEC SAMPLE

30.50.1

RDD 36 188C2, 189A5, 191B2, 180C2

30.50.1

DC 128 TR

RDD 128 183A3

RDD 22

DC 2 TR
DC 4 TR
DC 16 TR
189C2 SEL + READY MOD 4

30.51.1

END BKWD STOP DELAY 189A5

RDD 136

DC 8 TR
DC 128 TR
189C3 SEL + READY MOD 2 OR 4

30.55.1

RDD 38

DC 2 TR
DC 4 TR
DC 32 TR
189B3 SEL + READY MOD 2

30.52.1

RDD 110

LRCR ERROR SAMPLE 190C5

DC 2 TR
DC 4 TR
DC 8 TR
DC 32 TR
DC 64 TR
189C2 SEL + RDY 7330

181C2
WD 28
OR
RD-28

30.56.1

7330 RDD 110 183A3, 188A6, 188A3

RDD 64

DC 64 TR
189C3 SEL + READY MOD 2 OR 4

RDD 64 OR RDD 78 185B5

RDD 152

30.53.1

DC 8 TR
DC 16 TR
DC 128 TR
189C3 SEL + READY MOD 2 OR 4

RDD 152 OR RDD 2106 185A6, 188A3, 190B1

RDD 144

30.54.1

DC 16 TR
DC 128 TR

RDD 144 180C3 (NOTE 1)

RDD 2106

DC 2 TR
DC 8 TR
DC 16 TR
DC 32 TR
DC 2048 TR
189C2 SEL + RDY 7330

186B1 RESET
188B2 FWD STOP DLY D44
188B2 FWD STOP DLY D98
188D4 RDD 152 OR RDD 2106

RDD 144 RESET

181A6, 182A5, 183A3, 183A6
185A4, 185A5, 188C2, 188A3
188A6, 190B1

FORWARD STOP DELAY
30.56.1

IND
FWD STOP DELAY IND

FWD STOP DELAY
L
30.56.1

188B4 7330 RDD 110
188B3 RDD 144 RESET

FWD STOP DELAY 186A2

FSD 44

DC 4 TR
DC 8 TR
DC 32 TR
181C6 WRITE

FWD STOP DLY D44 188A3

FSD 98

DC 2 TR
NOT DC 4 TR
DC 32 TR
DC 64 TR
183C6 READ ONLY

FWD STOP DLY 98 188A3

182D2 MS SAMPLE

FSD 1

DC 1 TR
NOT DC 2 TR
NOT DC 4 TR
NOT DC 8 TR

COMPUTE 180C3 (NOTE 1)

CHECK CHARACTER LATCH
40.61.1

IND
CHECK CHAR IND

CHECK CHAR
L
40.61.1

188B5 RDD 36
188B3 RDD 144 RESET

CHECK CHAR 183A3, 180C3

NOT CHECK CHAR 183C3, 188A6, 191B5

NOTE 1: RESET THE TAPE IN PROCESS LATCH IN CONTROL UNITS.

FIGURE 188. TAU RDD, FSD AND CHECK CHARACTER

FIGURE 189. TAU GO AND TAPE DRIVE INPUTS

189 C3 SEL + READY MOD 2 OR 4 — AM
183 D3 READ COND — AM

FINAL AMPLIFIER CTRL
40.10

181C6 WRITE
180A3 AMPLIFIER BIAS
181C5 NOT WRITE
I
LO

185D3 D16Ø OR D2Ø48
188B3 RDD 144 RESET
GATE ON FINAL AMPS
L
30.52.1
181B1
AM

180A6 8VPP READ BUS 1 BIT 729
180A4 8VPP READ BUS 1 BIT 7330
AM
FILTER OUTPUT
1 BIT
AM

40.52.1

181C6 WR TM
182D3 WC 2
WRITE TM (NOTE 1)

181C6 NOT WRITE TM
192D2 NOT FREEZE R-W REG
WRITE GATE

186B1 RESET
182D3 WC 1
184D4 RC 6
181C2 WD 28 OR RD 28
RESET R-W REG

180B3 1 BIT WRITE DATA LINE

READ - WRITE REGISTER
40.50.1

183D3 READ COND ONLY

RW REG 1 BIT
L
40.50.1
IND
RW REG 1 BIT IND
RW REG 1 BIT 191A3 , 180C3
NOT RW REG 1 BIT 191A3

182C6 WRITE COND
D
WRITE BUS 1 BIT 729 180
D
WRITE BUS 1 BIT 7330 180

FINAL AMPLIFIERS
40.10.1

LO CLIP INPUT
LO
AM
LO CHAN 1 BIT 184 A6

REG A AND REG B BITS
40.20.1
B REG 1 BIT 191A6, 192A5
IND
B REG 1 BIT IND

B REG 1 BIT
L
40.20.1
NOT B REG 1 BIT 192A5

191C6 A REG VRC CHECK

192D2 NOT STOP ON ERROR

A REG 1 BIT 191A6 , 192A5 , 183C2
IND
A REG 1 BIT IND

HI
AM
HI CHAN 1 BIT 184 A6
HI CLIP INPUT

A REG 1 BIT
L
40.20.1
NOT A REG 1 BIT 191A6 ,192 ,183C2

184C3 WR RC-1Ø OR READ RC-7 RESET

191C6 NOT A REG VRC CHECK
184B4 WR RC-5 OR READ RC-7

1 BIT READ DATA LINE

INITIATE WR. DLY OR RD DLY
181C5

LONGITUDINAL REDUNDANCY CHECK REGISTER
50.40.1

IND
LRCR 1 BIT IND

LRCR 1
T
50.40.1

192B1 LRCR RESET

LRCR 1 BIT
LRCR 2 BIT
LRCR 4 BIT
LRCR 8 BIT
LRCR A BIT
LRCR B BIT
LRCR C BIT

50.42.1

188B4 LRCR ERROR SAMPLE
READ LRCR ERROR 192A2

LRCR 2 BIT
LRCR 4 BIT
LRCR 8 BIT
LRCR A BIT
LRCR B BIT
LRCR C BIT
192C2 ERROR CKT-2
181C2 WD-28 OR RD-28

NOTE 2

TURN ON GATE ON FINAL AMPLIFIERS LATCH

188D2 NOT CHECK CHARACTER
184B5 FIRST BIT
INITIATE WR DLY OR READ DLY
LRCR RESET
T
40.62
T
40.62
EVEN CHARACTER COUNT

NOTES
2. ONE POSITION OF SEVEN SHOWN
1 APPEARS ON 1, 2, 4 AND 8 BIT POSITIONS ONLY

FIGURE 190. TAU FINAL AMPLIFIERS

A REG VRC
50.10.1

A REG 1 BIT
NOT A REG 2 BIT
NOT A REG 1 BIT
A REG 2 BIT
A REG 4 BIT
NOT A REG 8 BIT
NOT A REG 4 BIT
A REG 8 BIT
190B4
A REG A BIT
NOT A REG B BIT
NOT A REG A BIT
A REG B BIT
A REG C BIT
183C2 NOT ODD REDUNDANCY
190B4 NOT A REG C BIT
183C2 ODD REDUNDANCY
I

CE PANEL
180A3 REG A ONLY
180A3 REG B ONLY

A REG VRC CHECK 190B4
NOT A REG VRC CHECK 190C4

184B4 WR RC-5 OR READ RC-7
188D2 NOT CHECK CHAR
185B6 NOT BACKSPACE
192B2 ERROR RESET
181C6 WRITE
180A2 EARLY SAMPLE (CE)

A REG VRC
L
50.51.1

IND
A REG VRC ERROR IND
WR A REG VRC CHECK 192A2
EARLY SAMPLE A REG VRC 192A2

READ WRITE REG VRC
50.20.1

RW REG 1 BIT
NOT RW REG 2 BIT
NOT RW REG 1 BIT
RW REG 2 BIT
RW REG 4 BIT
NOT RW REG 8 BIT
NOT RW REG 4 BIT
RW REG 8 BIT
190A6
RW REG A BIT
NOT RW REG B BIT
NOT RW REG A BIT
RW REG B BIT
RW REG C BIT
183C3 NOT ODD REDUNDANCY
190A6 NOT RW REG C BIT
183C3 ODD REDUNDANCY

188B5 RDD 36
181B5 NOT WRITE
188B6 RDD
184D5 RC 3
182D2 WC 9
192B2 ERROR RESET

RW REG VRC ERROR 192A2
R-W REG VRC
L
50.50.1
IND
RW REG VRC IND
RW REG ERR LATCH 192C2

ECHO ERROR
50.50.1

182D3 WC 4
NO ECHO
L
50.50.1
IND
NO ECHO IND
182D1 WC 14
ECHO ERROR 192A2
ECHO ERR
L
50.50.1
192B2 ERROR RESET
IND
ECHO ERROR IND
T80 WRITE ECHO 729 C
T80 ECHO PULSE 730 DT
192B2 ERROR RESET

FIGURE 191. TAU ERROR CIRCUITS I

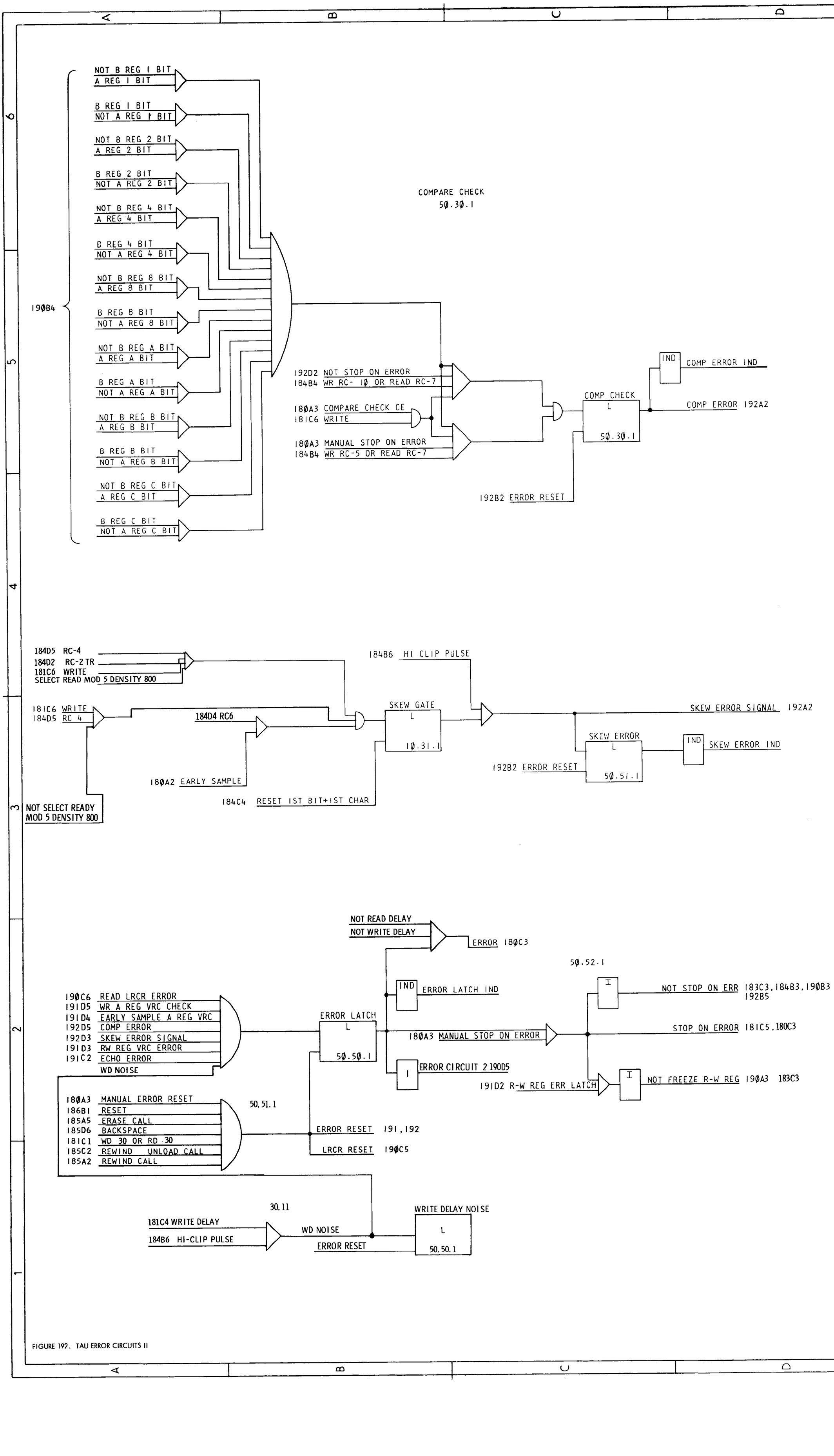


FIGURE 192. TAU ERROR CIRCUITS II

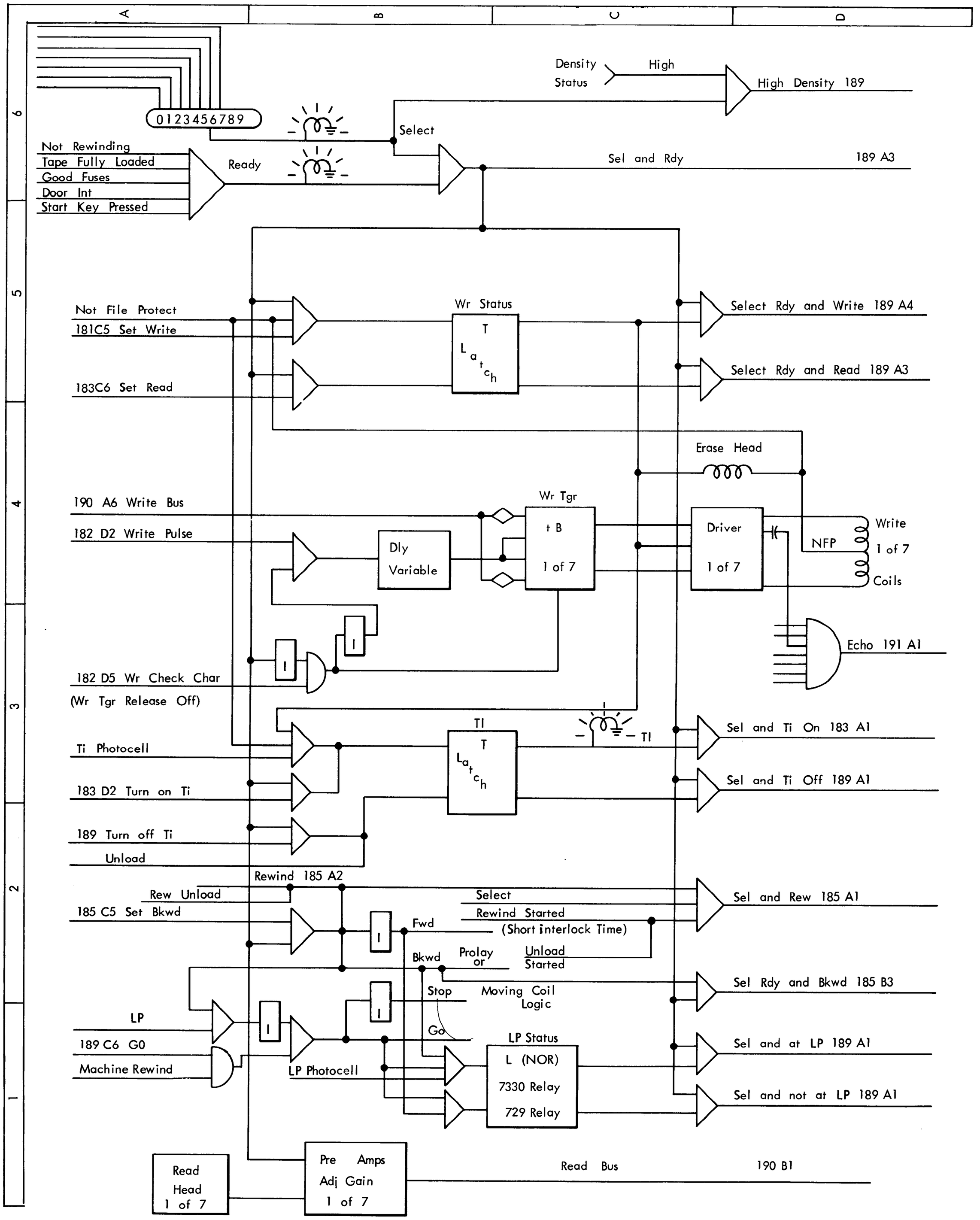


FIGURE T80. TAPE UNIT RESPONSE LOGIC

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15.62.04	44
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15.62.05	44
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15.63.05	44
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15.70.21	44
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15.70.23	44
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15.70.24	44
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ANY LAST INP CYC NOT 1401	27
AR BUS HP0B	16
AR BUS HP1B	16
AR BUS HP2B	16
AR BUS HP4B	16
AR BUS HP8B	16
AR BUS THP0B	16
AR BUS THP1B	16
AR BUS THP2B	16
AR BUS THP4B	16
AR BUS THP8B	16
AR BUS TP0B	16
AR BUS TP1B	16

OUTPUT LINES	FIG
H POS B INDEX TAG	21
H POS C INDEX TAG	21
H+Q OP.A CYC.ARING2	23
H+Q OP.A CYC.ARING4	23
HIGH	36
HIGH ADDER CARRY	37
HOLE COUNT ERROR	63
HOME PULSE	69
HOME RESET	69
HOME TRIG (RING)	68
I.CYCLE	04
I/O CHECK	28
I/O COMLAT LATCH	43A
I/O LAST EXECUTE	07
I/O LOAD OP CODE	39
I/O MOVE OP CODE	39
I/O PERC LATCH	43A
I OP	04
I 1	04
I 11	04
I 12	04
IAR GATE OUT U 0	10
INDEX AAR	11
INDEX GATE	11
INDEX NOT REQ	21
INDEX REQ	21
INH CHAR 0 WM BIT B1	49
INH CHAR 0 WM BIT D1	49
INHIBIT STKR	66
INPUT CYCLE GMWM INSERT	28
INPUT CYCLE.NOT LAST INPUT	27
INQ REQUEST LATCH	90
INQUIRY KEYBOARD UNLOCK	90
INSERT ZERO ON ADDR CH	21
INST RO GATE	11
INT END OF TRANSFER	46
INTERRUPT TEST OP CODE	39
INVALID CARD CODE (INTEG BFR)	63
J+R+I+X+0 OP CODES	40
J+R+X+I+0 OPS	40
K SYMBOL	38
KEYBOARD UNLOCK	88
L SYMBOL	38
LAST EXECUTE	07
LAST EXECUTE COND	41
LAST EXECUTE CYC * TLU	37
LAST INST RO CYCLE	08
LD CHR 0 ETC	49
LG EARLY B+S	02
LG EARLY F	02

OUTPUT LINES	FIG
LG SPECIAL A	02
LGA	01
LGA+R	02
LGA+T	02
LGB	01
LGB+C	02
LGB+S	02
LGC	01
LGC+T	02
LGD	01
LGD+E+F	02
LGD+U	02
LGE	01
LGE+V	02
LGF	01
LGF+W	02
LGG	01
LGH	01
LGJ	01
LGK	01
LGR	01
LGS	01
LGS+T	02
LGT	01
LGU	01
LGU+V+W	02
LGV	01
LGW	01
LGX	01
LGZ	02
LLG 1	03
LLG 2	03
LOAD MEM ON B CYC OP CODES	40
LOAD POINT (TAU)	80
LOW	36
LOW ADDER NO CARRY	37
LOZ SYMBOL	38
M OR L OP CODES	39
M SYMBOL	38
MAR TO IAR TTH8	10
MAR TO IAR U 0	10
MAR TTH 8 BIT	10
MAR TTH8 TO ADDR MOD	10
MAR U 0 BIT	10
MAR U 0 TO ADDR MOD	10
MASTER ERROR	58
MINUS ONE 01 LINE	17
MINUS ONE 28 LINE	17
MOD BY +1	18
MOD BY -1	18
MOD BY ZERO	18

OUTPUT LINES	FIG
MOVE ZERO SUP OP CODE	39
MPLY OP CODE	39
MQ LATCH	09
N SYMBOL	38
NEXT TO LAST AND LAST LOGIC GATE	03
NEXT TO LAST LG	03
NO BRANCH	42
NO BRANCH COND INTERRUPT	42
NO BRANCH OP CODES	39
NO C+D CYCLES OP CODE	40
NO CARRY LAT	31
NO D CYC AT I RING 6 OPS	40
NO INDEX ON 1ST ADDR OPS	40
NO NU A CH	37
NO NU ALPH	37
NO NU B CH	37
NO NU SPL CHAR	37
NO NUMERICS	37
NO OVERFLOW	35
NO SCAN	19
NO ZONES	37
NOT ADDR DOUBLE OP CODES	40
NOT AST FILL OR FLOAT DOLLAR	41.2
NOT ASTERISK	41.1
NOT ASTERISK FILL	41
NOT BLANK	41.1
NOT C CHAR	41.1
NOT COMMA	41.1
NOT CTRL 0	41.1
NOT DECIMAL	41.1
NOT DECIMAL CTRL	41.2
NOT DIV OVERFLOW	35
NOT DOLLAR SIGN	41.1
NOT EVEN HDRD ADDR	18
NOT LAST I CYCLE B	06
NOT MINUS SYMBOL	41.1
NOT PERC TYPE OP CODE	40
NOT R CHAR	41.1
NOT SIG DIGIT	41.1
NOT SOME SCAN	61
NOT SPACE (NOT AMPERSAND)	41.1
NOT ZERO BALANCE LATCH	35
NOT ZERO SUPPRESS	41.2
NOT 0 SUPPRESS	41.2
NUM 1 THRU 7	41.1
NUM 8 OR 9 CHAR	41.1
ONE SYMBOL	38
OP MOD BIT COMBINATIONS	38
OP MOD C BIT	26
OP MOD CHAR TIME * ARS	26

OUTPUT LINES	FIG
AR BUS TP2B	16
AR BUS TP4B	16
AR BUS TP8B	16
AR BUS TTHP0B	16
AR BUS TTHP1B	16
AR BUS TTHP2B	16
AR BUS TTHP4B	16
AR BUS TTHP8B	16
AR CH VC GROUP ONE	24
AR CH VC GROUP TWO	24
AR EXIT CH C BIT	24
AR EXIT CH 1 BIT	24
AR EXIT CH 2 BIT	24
AR EXIT CH 4 BIT	24
AR EXIT CH 8 BIT	24
AR TTH 8 TO ADDR EXIT	10
AR U 0 TO ADDR EXIT	10
ARITH TYPE OP CODES	39
ARS D+T OP CODES	40
ARS L+M+T OP CODES	39
ARS NO OP	39
ASSM CH A BIT	29
ASSM CH A BIT INSERT	28
ASSM CH A+B BITS	29
ASSM CH B BIT	29
ASSM CH C CHAR BIT	28
ASSM CH NOT A BIT	29
ASSM CH NOT B BIT	29
ASSM CH NOT C CHAR BIT	28
ASSM CH NOT WM BIT	28
ASSM CH NOT 1 BIT	29
ASSM CH NOT 2 BIT	29
ASSM CH NOT 4 BIT	29
ASSM CH NOT 8 BIT	29
ASSM CH NU ONE INSERT	28
ASSM CH NU ZERO INSERT	30
ASSM CH WM BIT	28
ASSM CH 1 BIT	29
ASSM CH 2 BIT	29
ASSM CH 4 BIT	29
ASSM CH 8 BIT	29
ASTERISK	41.1
ASTERISK FILL	41.2
ASTERISK OR $ SIGN	41.1
ASTERISK SYMBOL	38
AUTO SPACE LATCH	71
AUX BIN ADDER 4 BIT	56
AUX BIN ADDER 8 BIT	56
B CH BITS	25
B CH INSERT PLUS ZERO	30
B CHAR SEL ERROR	59
B CYC FIRST OP CODES	40
B CYCLE	05
B DATA REG RESET	48
B DATA REG WM BIT	50
B REG RESET ERROR	59
B SYMBOL	38
B TO LAST LG	02
BACKWARD (TAU)	80
BAR GATE OUT U 0 BIT	12
BIN REG A1 BIT	54
BIN REG A2 BIT	54
BIN REG A4 BIT	54
BIN REG A8 BIT	54
BIN REG B4 BIT	54
BIN REG B8 BIT	54
BIN REG NOT B4 BIT	54
BIN REG NOT B8 BIT	54
BIT GEN OUT (INTEG BFR)	63
BIT TEST BRANCH OP CODE	39
BLANK	41.1
BLANK OR ZERO	41.1
BLANK SYMBOL	38
BLANK 0 COMMA	41.1
BLANK 0 PUNC OR SIG DIGIT	41.1
BLANKED CR SYMBOL	41
BLANKED ZERO + COMMA	41
BODY LAT	09
BR ON STATUS CH 1	39
BR ON STATUS CH 2	39
BRANCH TO AAR	42
BRANCH TO 00001	42
BUFFER BUSY TO CHAN BUSY .PUN.	61
BUFFER BUSY TO CHAN BUSY .RDR.	62
BUFFER STROBE TO C.P.U.	66
BUSY (TAU)	78
B0.B1 SHIFT	33
B0 SHIFT	33
B1 SHIFT	33
B2 + B3 SHIFT	33
B2 SHIFT	33
B3 SHIFT	33
C CYCLE	06
C CYCLE OP CODES	40
C OR R OR MINUS	41.1
C SYMBOL	38
CAR GATE OUT U 0 BIT	13
CARRIAGE BUSY	71
CARRIAGE GO	71
CARRIAGE STOPPED	71
CARRY LATCH	31
CC REG RESET	71
CE GO	67
CE PUNCH XFER GATE	67
CE RD XFER GATE	67
CE RING CK (INTEG BFR)	67
CH I OVLP	43
CH I UNOVLP	43
CHAIN HOME	69
CHAR TEST BR OP CODE	39
CHECK CHAR (TAU)	81
CLEAR OP CODE	39
CLEAR WM OP CODE	39
CLOCK STOPPED	01
CLOCKED STROBE	44
CMP MODE B CYCLE	37
CMP MODE SET A CYC CTRL	37
CMP OP CODE.1ST SCAN	31
COML AT OP OR 9 SYMBOL OP MOD	53
COML AT SIGN	38
COMMA	41.1
COMMON OP CODE GROUPING	39
COMPARE EQUAL	36
COMPARE HIGH	36
COMPARE LOW	36
COMPARE OP CODE	39
COMPARE TGR (1403)	69
COMPAT TSLTR THP 0 BIT	57
COMPAT TSLTR THP 1 BIT	57
COMPAT TSLTR THP 2 BIT	57
COMPAT TSLTR THP 2 BIT	57
COMPAT TSLTR THP 4 BIT	57
COMPAT TSLTR THP 8 BIT	57
COMPAT TSLTR THP 8 BIT	57
COMPAT TSLTR TTHP 0.1 BITS	57
COMPAT TSLTR TTHP 0.1 BITS	57
COMPAT TSLTR TTHP 2.8 BITS	57
COMPAT TSLTR TTHP 2.8 BIT	57
COMPL ADDA	31
COMPL ADDB	31
COMPL LATCH	31
COMPUTE (TAU)	81
COMPUTE DISABLE CY	46
COND TEST BR OP CODE	39
CONS BACKSPACE	88
CONS CARR RTN	88
CONS CHK STROBE	85
CONS CY LATCH RST	85
CONS CYCLE LATCH SET	85
CONS CYCLE START	89
CONS CYCLE START CND	89

OUTPUT LINES	FIG
OP MOD NOT C BIT	26
OP MOD NOT 1 BIT	26
OP MOD REG	60
OP MOD SYMBOL FOR I/O STATUS	38
OP MOD TO A CHAN B CYC OP CODES	40
OP MOD 1 BIT	26
OP REG ARS C BIT	26
OP REG ARS NOT C BIT	26
OP REG C BIT	26
OP REG COM NOT C BIT	26
OP REG CON C BIT	26
OP REG NOT 1 BIT	26
OP REG SET ERROR	59
OP REG 1 BIT	26
OP REG 1401 C BIT	26
OP REG 1401 NOT C BIT	26
OUTPUT CYCLE	43A
OUTPUT WM CYCLE	28
OVERFLOW	35
P SYMBOL	38
PARITY 1 (INTEG BFR)	63
PARITY 2 (INTEG BFR)	63
PERC SYMBOL	38
PERCENT TYPE OP CODES	40
PLUS ONE 18 LINE	17
PRINT BUFFER BUSY	51
PRINT CHECK (1403)	71
PRINT ERROR LATCH	70
PRINT IN PROCESS LTCH	71
PRINT SCAN 49	69
PROCESS ROUTINE	87
PROGRAM RESET	51
PROGRAM SET BR CTRL	89
PRT LOCKED CND PROCEED	88
PRTR LAST COL	91
PSS 1,2 + 3 (1403)	69
PUNCH BIT GEN (INTEG BFR)	63
PUNCH BUSY TO PRIORITY CKTS	45
PUNCH DECODE	62
PUNCH FEED GATE	67
PUNCH PRIORITY REQ	66
PUNCH SCAN TO TIME PULSE 1 LATCH	61
PUNCH STACKER	61
PUNCH XFER REQ	66
Q + V SYMBOL OP MOD	38
Q SYMBOL	38
Q SYMBOL	38
Q2.B0+B2 SHIFT	34
Q2.B1+B3 SHIFT	34
Q6.B0 SHIFT	34

OUTPUT LINES	FIG
Q6.B1 SHIFT	34
Q6.B2 SHIFT	34
Q6.B3 SHIFT	34
Q8.B0.B1 SHIFT	33
Q8.B2+B3 SHIFT	33
R SYMBOL	38
R-W REG 1,2,4,8,A,B,C BITS (TAU)	84
RC-3 (TAU)	79
RD ENCODER (INTEGER)	62
RD XFER REQ	61
RD PRIORITY REQ	61
RDD (TAU)	81
RDD-144 (TAU)	81
RDD-36 (TAU)	81
RDR READY TO C.P.U.	45
RDR STACKER	64
READ CALL 1411 MEM	02
READ IN	68
READ OUT BAR	44A
READ REQUEST	61
READ SCAN	61
READ 1ST ADDRESS TO A.CAR	11
READER BUSY TO PRIORITY CKTS	62
READER READY	61
READY TO BUFFER	43
RECORD MARK	38
REGEN CHR 0 ETC	49
REGEN COMPL	30
REGEN MEM ON B CYC OPS	40
REGEN TRUE	30
REGEN UNITS-BODY	08
RESET ADD OP CODE	39
RESET BAR	44A
RESET E 1 FULL	44
RESET E2 FULL LATCH	44
RESET OP MOD REG	26
RESET SUB OP CODE	39
RGEN COMPL	30
RING ADV (PTR)	66
RING ADVANCE (INT BUFF)	61
RNG CHECK (INTEG BFR)	76
RO AAR ON A CYC OPS	40
RO BAR ON SCN B CYC OPS	40
RO FIXED ADDR	21
RO 00001 INDEX ADDR	21
RO 00101 INDEX ADDR	21
RO 00201 INDEX ADDR	21
S SYMBOL	38
SCAN CALL (PRINTER)	65
SCAN TRIG.	68

OUTPUT LINES	FIG
SEL + TI ON (TAU)	79
SEL AND NOT LP ()AU)	83
SEL AND RDY H1 7330	83
SEL AND READY MOD4 (TAU)	83
SEL AND REWIND	80
SEL AND TI OFF	83
SEL CHR 0 ETC	49
SELECT UNIT 1	45
SELECT UNIT 2	45
SELECT UNIT 4	45
SENSE STROBE	48
SET A RING 1 TGR	22
SET ASTERISK	28
SET ASTERISK A CH CHECK CTRL	28
SET BAR	44A
SET CARRY LATCH	30
SET COMPL CTRL LATCH	30
SET E1 REG	44
SET E2 FULL	44
SET GM	28
SET HIGH CYCLE	37
SET NO CARRY	30
SET OP MOD REG	26
SET OP REG	59
SET TRUE	30
SET WM	41
SET WM OP CODE	39
SET X CYC CTRL A	22
SIG DIGIT	41.1
SLASH SYMBOL	38
SPACE (AMPERSAND)	41.1
SPACE OR SKIP CTL	71
SPEC CHAR C CONSOLE	87
SPEC CHAR E CONSOLE	87
SPEC CHAR S CONSOLE	87
SPL CHAR + NO NU	37
SPL CHAR A CH	37
SPL CHAR ALPH	37
SPL CHAR B CH	37
SPL CHAR NO NU	37
START COMP ADD 1	30
START COMP ADD2	30
START COMP INDEX	30
START FORMS OP	69
START KEY	87
START KEY PULSE	87
START TRUE ADD 1	30
START TRUE ADD 2	30
START TRUE INDEX	30
START 1401 INDEX	30
STATUS SMP A	46

OUTPUT LINES	FIG
CONS ERROR CTL	91
CONS GATE POS 30	86
CONS INQUIRY MX GATE	90
CONS MOVE READ OP	90
CONS MOVE WRITE OP	90
CONS MX ADDR DR	91
CONS MX X1A	86
CONS MX Y1,Y2 ETC	86
CONS MX 32	90
CONS MX 32 OR 33	90
CONS OUTPUT ERR	91
CONS OUTPUT 2 BIT	89
CONS OUTPUT 4 BIT	89
CONS PRG PRT OUT MX GATE	90
CONS PRINTER NOT BUSY	85
CONS PRINTER NOT BUSY SET	85
CONS PRINTER SHIFT COMPLETE	88
CONS PRINTER STROBE	90
CONS READ OP	90
CONS SET START CND	87
CONS SPACE	88
CONS STOP CR COMPLETE	87
CONS STOP PRINT COMPLETE	87
CONS STROBE GATE	90
CONSOLE OUTPUT A BIT	90
CONSOLE OUTPUT B BIT	90
CONSOLE OUTPUT C BIT	90
CONSOLE OUTPUT 1 BIT	90
CONSOLE OUTPUT 8 BIT	90
CONSOLE STROBE	90
CONSOLE WRITE OP	90
CONTROL REG DISABLE	26
CORRECT TRANSFER TO BFR.	43B
CREDIT + NOT UNIT CONTROL CHAR	41
CTRL ZERO	41.1
D CYCLE	06
D SYMBOL	38
DAR GATE OUT U 0 BIT	14
DATA MOVE A CYC CTRL SET	05
DATA MOVE OP CODE	39
DECELERATE (1403)	71
DECIMAL	41.1
DECIMAL CTRL	41.2
DISCONNECT CALL	46
DIV OP CODE	39
DIV OVERFLOW	35
DOLLAR SIGN	41.1
DOLLAR SIGN SYMBOL	38
E CH ANY STATUS ON	45.3
E CH BUSY	45

OUTPUT LINES	FIG
E CH CHECK	45.2
E CH CLR	45.3
E CH COND	45.2
E CH DISC LATCH	46
E CH DISCON TO 1301	46
E CH DISCON TO 1405	46
E CH END OF RECORD	46
E CH EXT END TRAN	46
E CH FORMS CTRL OP	39
E CH IN PROCESS	43B
E CH INPUT MODE	43A
E CH INTERLOCK	43A
E CH INT END OF TRF	46
E CH LOAD MODE	43A
E CH MOVE AND LOAD MODE	43A
E CH NO STATUS ON	45.3
E CH NO TRANSFER	45.3
E CH NOT READY	45
E CH OUTPUT MODE	43A
E CH READY A,B	46
E CH READY B (E CYCLE REQUIRED)	46
E CH READY BUS	45
E CH READY C (E CYCLE REQUIRED)	46
E CH READY TO BUFFER	44A
E CH STACKER SEL OP	39
E CH STATUS SMP A	46
E CH STATUS SMP A DELAY	46
E CH STATUS SPL B	46
E CH STATUS SPL B DLY	46
E CH TAPE CALL	43B
E CH UNGATED SMP A	46
E CH UNOVLP OVLP	43A
E CH WLR	45.3
E CH 2 CHAR ONLY	40
E CH 2ND SPL B	46
E CHANNEL	43A
E CYCLE	44A
E CYCLE REQUIRED	46
E OP . B CY	41.1
E OP.B CYCLE 1ST SCAN	41
E OR Z OP . B CY	41.1
E SYMBOL	38
E 2 REG 1 BIT	44
E+Z.2D SCN EXTENSION	41
E+Z.3D SCN EXTENSION	41
EAR GATE OUT U 0 BIT	15
EARLY B	02
EARLY F	02
EARLY LAST GATE I/O	02
EARLY S	02

OUTPUT LINES	FIG
EDIT OP CODE	39
EDIT SET A CYC CTRL	05
EDIT SET B CYC CTRL A	05
EDIT SET B CYC CTRL C	41
EDIT SET B CYC CTRL D	41
EDIT SET B CYC CTRL E	41
EDIT SET B CYC CTRL F	41
EDIT SET B CYC CTRL G	05
EDIT SKID CYCLE	41
EMITTER (PRINTER)	71
ENCODE	61
ENCODE A (INTEG BFR)	62
ENCODE B (INTEG BFR)	62
ENCODE C (INTEG BFR)	62
ENCODE 1 (INTEG BFR)	62
ENCODE 2 (INTEG BFR)	62
ENCODE 4 (INTEG BFR)	62
END OF CHAR RESET	85
END OF RECORD L.	46
END OF SCAN(INTEG BFR)	61
EQUAL	36
EQUAL COMPARE (1403)	69
EQUAL LOW LATCH RESET	36
EQUAL LOW LATCHES SET	36
ERROR (TAU)	82
ERROR SAMPLE	58
ERROR 1 (1403)	70
ERROR 2 (1403)	70
EVEN HDRD ADDR	18
EXCLAM MARK	38
EXTENSION LATCH	09
E1 REG FULL	44
E1 REG WD SEP	44
E2 FULL	44
E2 WD SEP	44
F SYMBOL	38
FAR GATE OUT U 0 BIT	15
FAST SKIP CTL	71
FIVES ADV	65
FIVES RING	68
FLOAT DOLLAR SIGN	41.2
FORMS + 1403 PRT BUF BUSY	51
FORMS BUSY STATUS	45
G OP . C CYCLE	27
G OP SET C CYC CTRL B	06
G SYMBOL	38
GATE ON PRT SCAN CALL (INTEG BFR)	67
GATE ON R.I. TGR.	67
GO	43B
GROUP MARK	38
H POS A INDEX TAG	21

OUTPUT LINES	FIG
STD A CYC OPS.A CYC	39
STOP AT F TLU	37
STOP AT F ON B CYC OP CODES	40
STOP AT H ON B CYC OPS	40
STOP AT J TLU	37
STOP AT J ON B CYC OP CODES	40
STOP.BRANCH OP CODE	39
STOP KEY LATCH	87
STOP LATCH	87
STOP ON ERROR (TAU)	82
STOP PGM RES CARRIAGE RET	87
STOPPED.NOT IN PROCESS	01
STOPPED AT CYCLE END	89
STOR AR SET C CYC CTRL A	06
STOR AR SET C CYC CTRL B	06
STOR SCN LOAD	03
STORE ADDR REG OP CODE	39
STORE AR SET A CYC CTRL A	05
STORE AR SET A CYC CTRL B	05
STROBE	66
SUBT OP CODE	39
SYNC CHK LATCH	70
T POS A INDEX TAG	21
T POS B INDEX TAG	21
T POS C INDEX TAG	21
T SYMBOL	38
TABLE SEARCH OP CODE	39
TENS ADV (1403)	65
TENS RING 0 THRU 9	68
TENS 0,3 ETC (1403)	65
TEST PRINT ERRORS	53
TEST PUNCH ERRORS	53
TEST READ E OF F	53
THREES ADV	65
THREES RING	68
TILT + ROTATE (731)	85
TIME GATE (INTEG BFR)	61
TIME PULSE 1 + 2	61
TIME PULSE 2	61
TRUE ADD B	31
TRUE ADDA	31
TWO ADDR OP CODES	40
TWO SYMBOL	38
U SYMBOL	38
UNIT CONTROL OP CODE	39
UNITS + BODY LATCH	36
UNITS + TENS RING (INTEG BFR)	61
UNITS LATCH	08
USE A CH NUM	27
USE A CH WM	27
USE A CH ZONES	27
USE ADDER NU	30
USE B CH NUM	27
USE B CH WM	27
USE B CH ZONES	27
USE NO NUMERICS	27
USE NO WM	27
USE NO ZONES	27
V SYMBOL	38
VALIDITY CHECK (INTEG BFR)	63
W + X SYMBOL OP MOD	38
W OR V OP CODES	40
W SYMBOL	38
W TYPE BRANCH CONDITION	43
WC 2 ETC (TAU)	78
WD 320 + WD 1088 (TAU)	78
WD 49 (TAU)	78
WM OP.A CYCLE	05
WM PERIOD LATCH	91
WM+E+Z+W+V+/+. OPS	40
WORD MARK OP CODES	39
WR RC-5 OR READ RC 7 (TAU)	79
WRITE (TAU)	78
WRITE B+SPEC CHAR	41
WRITE CALL 1411 MEM	03
WRITE COND (TAU)	78
WRITE EDIT ASTERISK	41
WRITE EDIT BLANK	41
X CYCLE	06
X RD	48
X SYMBOL	38
X SYMBOL GATED	38
X WR	48
Y RD	48
Y SYMBOL	38
Y WR	48
Z OP . B CY	41.1
Z OP SET A CY CTRL	05
Z PULSE	48
Z SYMBOL	38
ZERO BALANCE LATCH	35
ZERO OR DECIMAL	41.1
ZERO SUPPRESS	41.2
ZN OR WM TEST BRANCH OP CODE	39
ZONE ADDER A. NOT B. NOT C	55
ZONE ADDER A.B.C	55
ZONE ADDER A.B.C	55
ZONE ADDER A.NOT B.NOT C	55
ZONE ADDER CARRY	55
ZONE ADDER NOT A.B.NOT C	55
ZONE ADDER NOT A.B.NOT C	55
ZONE ADDER NOT A.NOT B.C	55
ZONE ADDER NOT A.NOT B.C	55
ZONES (COMPARE)	37
0 OR DECIMAL	41.1
0 SUPPRESS	41.2
1 ADDR PLUS OP MOD OP CODE	40
1ST CP	01
1ST I/O CYCLE CONTROL	51
1ST SCAN	19
1ST SCN FIRST OP CODE	39
1401 . I CYCLE	26
1401 .C OP. I RING 4 TIME	36
1401 .I CYCLE.I RING 5 + 10	57
1401 .X CYCLE.A RING 4 TIME	57
1401 LB + Q + H OP CODE	39
1401 B OP CODE	52
1401 BRANCH LAST EX CYCLE	53
1401 BRANCH LATCH	53
1401 CARD OR PRINT OP CODE	52
1401 CARD PR ERR SAMPLE	51
1401 CARD PRINT ERROR	51
1401 CARD PRINT IN PROCESS	51
1401 CD/PRT ERROR	60
1401 CHAR TEST OP CODE	52
1401 COND TEST OP CODE	52
1401 D OP CODE	52
1401 D+P+Y OP	52
1401 DATA MOVE OP	52
1401 DATE MOVE SET OP MOD	26
1401 H+Q. A CYCLE	27
1401 I/O END POS	51
1401 I/O LOAD OP	52
1401 I/O MOVE OP	52
1401 I/O SET BRANCH CNDS	51
1401 I RING 5 OR 10 TIME ICY	55
1401 I RING 8 BRANCH OP	52
1401 I RING 9 BRANCH OP	52
1401 I-CYC NEXT	08
1401 MODE	52
1401 MODE	52
1401 MODE.ARING 4.X CYC	03
1401 MODE.I RING 5+10.I CYC	03
1401 NO EXE CY BRANCH OP	52
1401 NOP LIROC	52
1401 P OP CODE	52
1401 PCH/PRT ERROR	60
1401 POUND SIGN OP CODE	52
1401 PRINT	51
1401 PUNCH	51
1401 PUNCH PRINT ERROR	51

OUTPUT LINES	FIG
1401 Q OP TRANS	05
1401 READ	51
1401 STOP AND WAIT	53
1401 STORE AAR OP CODE	52
1401 STORE AR OPS	39
1401 STORE AR.C CYCLE	27
1401 STORE BAR OP CODE	52
1401 TAKE I TO B CYCLE	53
1401 Y OP CODE	52
1403 PRINTER BUFFER BUSY	51
2 ADDR NO MOD OP CODE	40
2 ADDR PLUS OP MOD OP CODES	40
2 CHAR ONLY	40
2 D CONDITION A BRANCH	43
2D CP 3	02
2D SCAN	19
2D SCN SIG CHAR	41
3D SCAN	19
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